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DESIGN AND DEVELOP A

MOS MAGNETIC MEMORY

FINAL REPORT

11 March 1966 through 31 January 1967

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1.0 FOREWORD

This is the final technical report for the work performed under contract NAS8-20594, covering the period beginning 11 March 1966 and ending 31 January 1967. The contract was under the technical direction of Mr. G.A. Bailey of the Applied Research Branch of the Astrionics Laboratory, NASA, Marshall Space Flight Center.

2.0 REVIEW OF OBJECTIVES

The objective of this program was to determine the interface problems which exist between plated wire memories and MOS (metal-oxide-silicon field effect transistor) memory electronics. During the study phase of the contract period the interface problems were defined and means for reducing or eliminating them discussed. A feasibility breadboard memory system was fabricated to demonstrate the use of MOS transistors for interfacing directly with a plated wire memory.

3.0 INTRODUCTION

Metal oxide semiconductor (MOS) integrated circuitry has been heavily investigated as a means of producing low cost, low power, highly reliable digital computer logic circuits.

Plated wire elements have been investigated in a similar manner to produce the identical goals within the memory area.

While these separate efforts have proven successful, the large gray area of memory electronics remained untouched. This interface area has been thoroughly investigated during the study phase of this contract and it has been shown feasible to design the memory electronics with MOS devices. A spaceborne computer constructed of MOS circuitry and a plated wire memory can provide considerable improvement in reliability over present day computers.

The interface problems between plated wire memories and MOS devices were determined, and solutions to these problems investigated and evaluated. The most important interface areas are:

1. Package compatibility between the plated wire stack and the MOS devices.

2. Interconnection of the memory and MOS devices.

3. Interconnection of the various MOS functional blocks.

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4. Total reduction of interfaces and interface connections.

5. Manufacturing compatibility of the plated wire and the MOS devices.

6. Power and speed requirements.

Each of these areas is discussed in detail in the following sections of this report.

Brief descriptions of the plated wire element and the MOS devices are contained in the following paragraphs.

3.1 Plated Wire

A plated wire memory element consists of a plated wire with an orthogonal current drive strap, as shown in Figure 1. Since the magnetic film has a preferred orientation of magnetization in the circumferential or easy direction, and exhibits a rectangular hysteresis loop, the two remanent storage states are oriented either clockwise or counterclockwise. In the axial or hard direction, the magnetization is reversible and linear.

During the READ mode a current passed through the word strap produces a field which is parallel to the hard axis. This field rotates the stored remanent magnetization from its circumferential direction into alignment with the hard axis thereby inducing a voltage in the bit wire, which functions as a sense line during the read operation. The polarity of the induced voltage is dependent upon the direction of the remanent state. When the word field is less than the film anisotropy, H_k, the removal of the word current will permit the magnetization vector to fall back to its original position. This constitutes a nondestructive readout (NDRO).

The conditions necessary for magnetization reversal by the application of circumferential and axial fields to result in an NDRO memory may be understood by referring to Figure 2. This figure is the Stoner-Wohlfarth astroid[1] as corrected for the existing conditons of nonpure rotational switching. Outside the astroid, reversible switching occurs. In between are areas where the switching mechanism is not clearly defined, and the extent of this area is a measure of the quality of the film. The smaller the area, the better the film. For NDRO operation, the orthogonal components (h_w and h_b) of the applied field H must each be within the NDRO zone, and their simultaneous vector sum must also not exceed the inner curve of the astroid. Not shown in Figure 2 are the effects of

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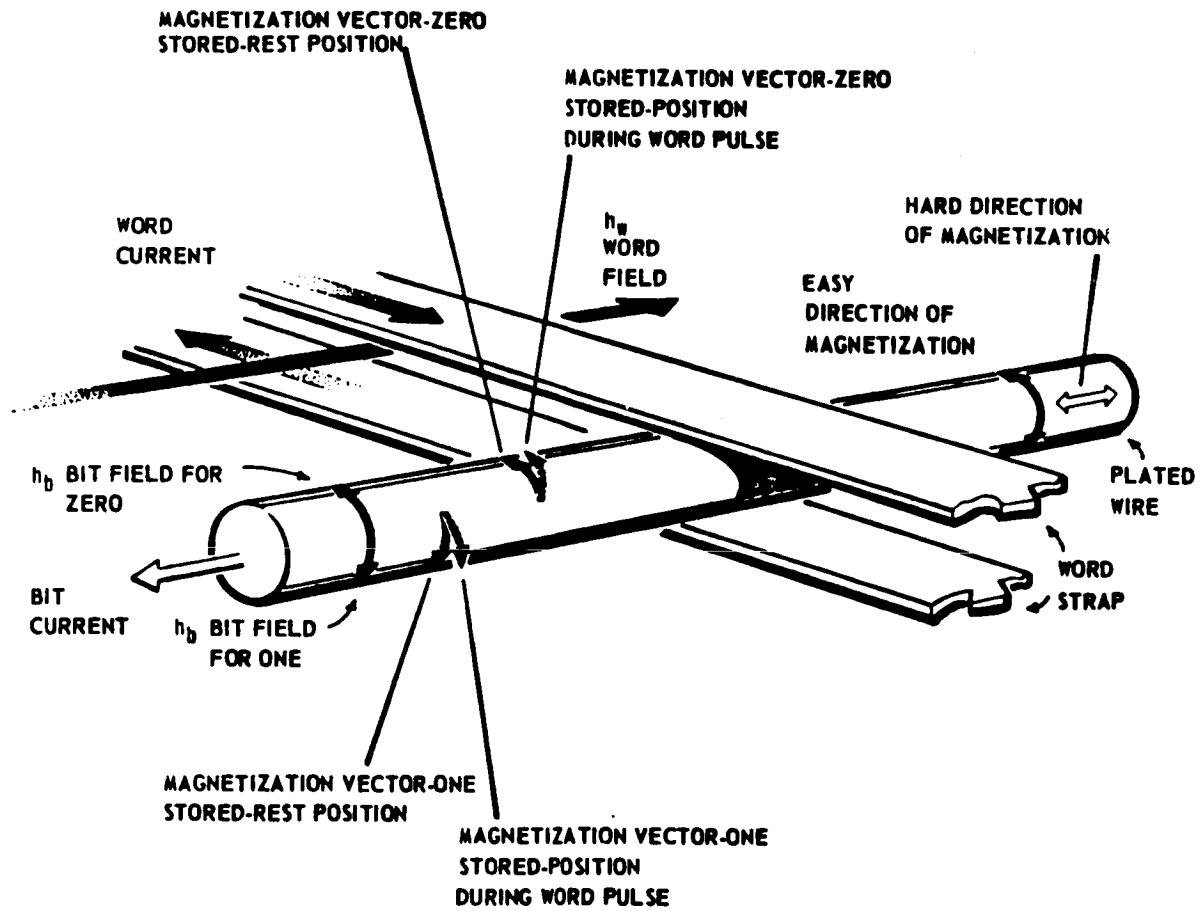
FIGURE 1. INFORMATION STORED ON PLATED WIRE
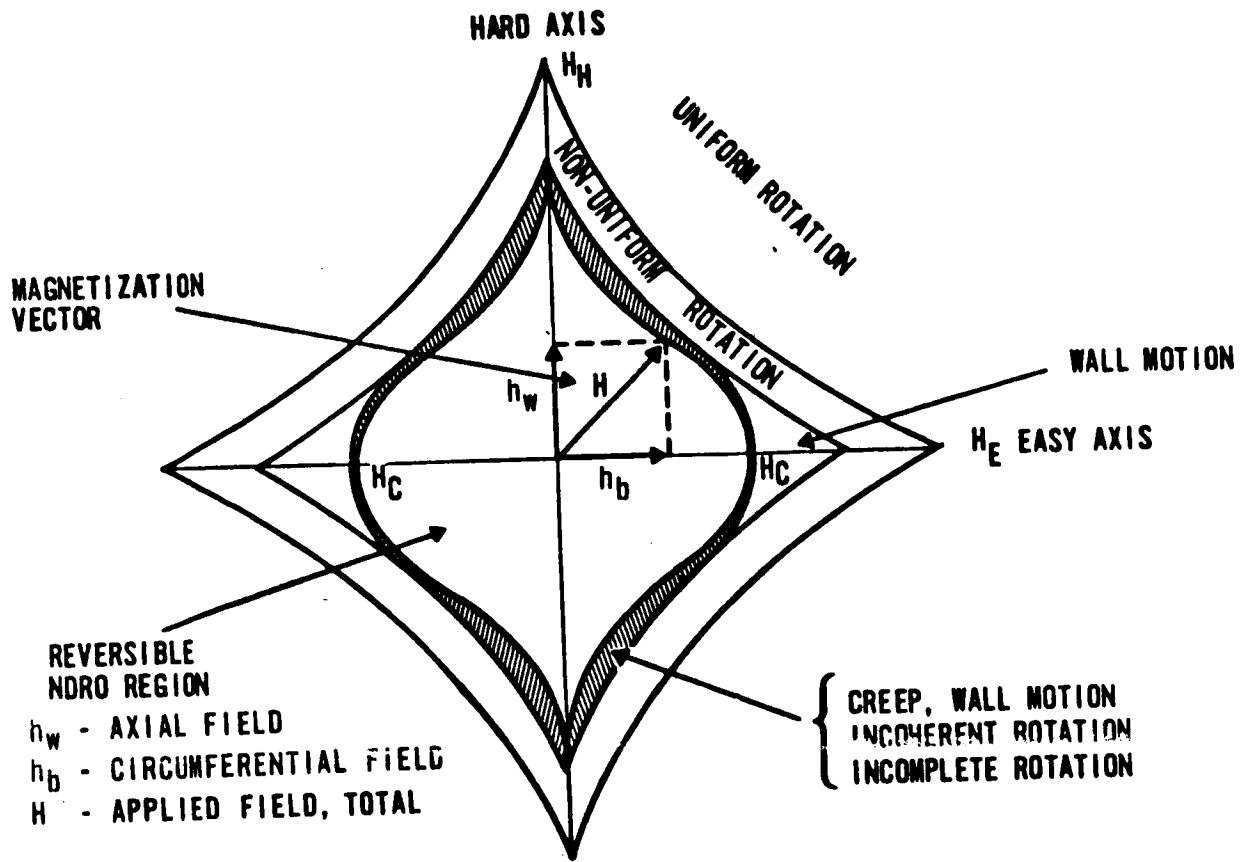
FIGURE 2. STONER-WOHLFARTH ASTROID

skew and dispersion which occur to some extent with all films. Skew is the term used for the angle between the easy axis distribution median value and some reference direction, while angular dispersion refers to the angular dispersion around this median. Both these effects are undesirable, and in effect reduce the effective working area for reversible switching.

The output of a single plated wire bit is shown in Figure 3.

During the WRITE mode the bit current produces a circumferentially oriented field. This field, when applied in coincidence with the word field, will incline the magnetization in an axial magnitude and polarity of the bit field. Subsequent removal of the word field aligns the net magnetization in the proper bit field direction. The removal of the bit field then completes the write cycle.

Figure 4 illustrates the write switching cycle using the idealized hysteresis loops of the easy and hard directions. The outer large loop results from solely applying a bit current, and is the easy direction loop. The inner linear curve results from the application of only an axial or word field. The remaining third curve represents the magnetization characteristics when both an axial and circumferential field are applied.

Assuming an initial condition of remanence at point 1, a circumferential bit field (H_b), less than the disturb value (H_d), is applied resulting in a flux change to point 2. With the addition of an axial field (H_w), less than the film anisotropy field (H_k), the magnetization vector is inclined in a direction established by the resultant field (H_r). This is indicated by a flux change to point 3 on the inner loop. Removal of the axial field aligns the magnetization in the circumferential direction established by the bit field, and is shown as point 4 on the easy direction loop. Subsequently, the circumferential field is removed and point 5 represents the new remanent flux state. Flux reversal from point 5 to point 1 can be described in an identical manner.

3.2 MOS Devices

Switching circuits are normally designed with enhancement mode MOS transistors. These devices are normally off with zero gate voltage; therefore, they act as on-off switches and require only a single supply voltage.

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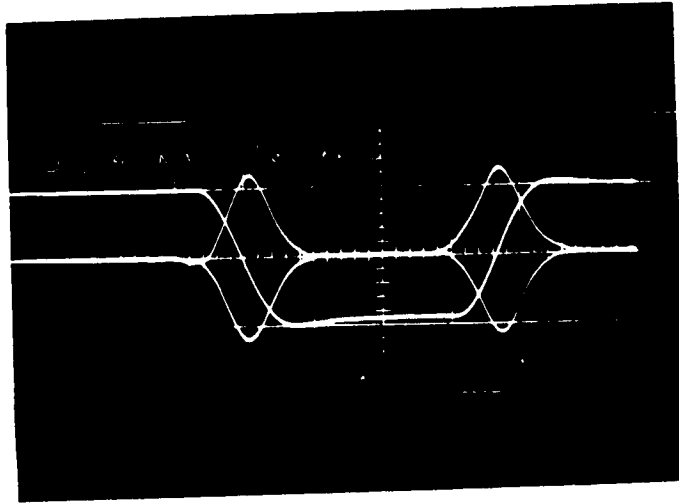
SWITCHING CURRENT & VOLTAGE OUTPUT:
1 BIT: PLATED WIRE
$I\omega$ - WORD CURRENT: ma
V_0 - VOLTAGE OUTPUT: mv

HORIZONTAL SCALE: 50 nsec/DIVISION
VERTICAL SCALE: 5 mv/DIVISION

FIGURE 3.   CURRENT AND VOLTAGE OUTPUT
OF PLATED WIRE
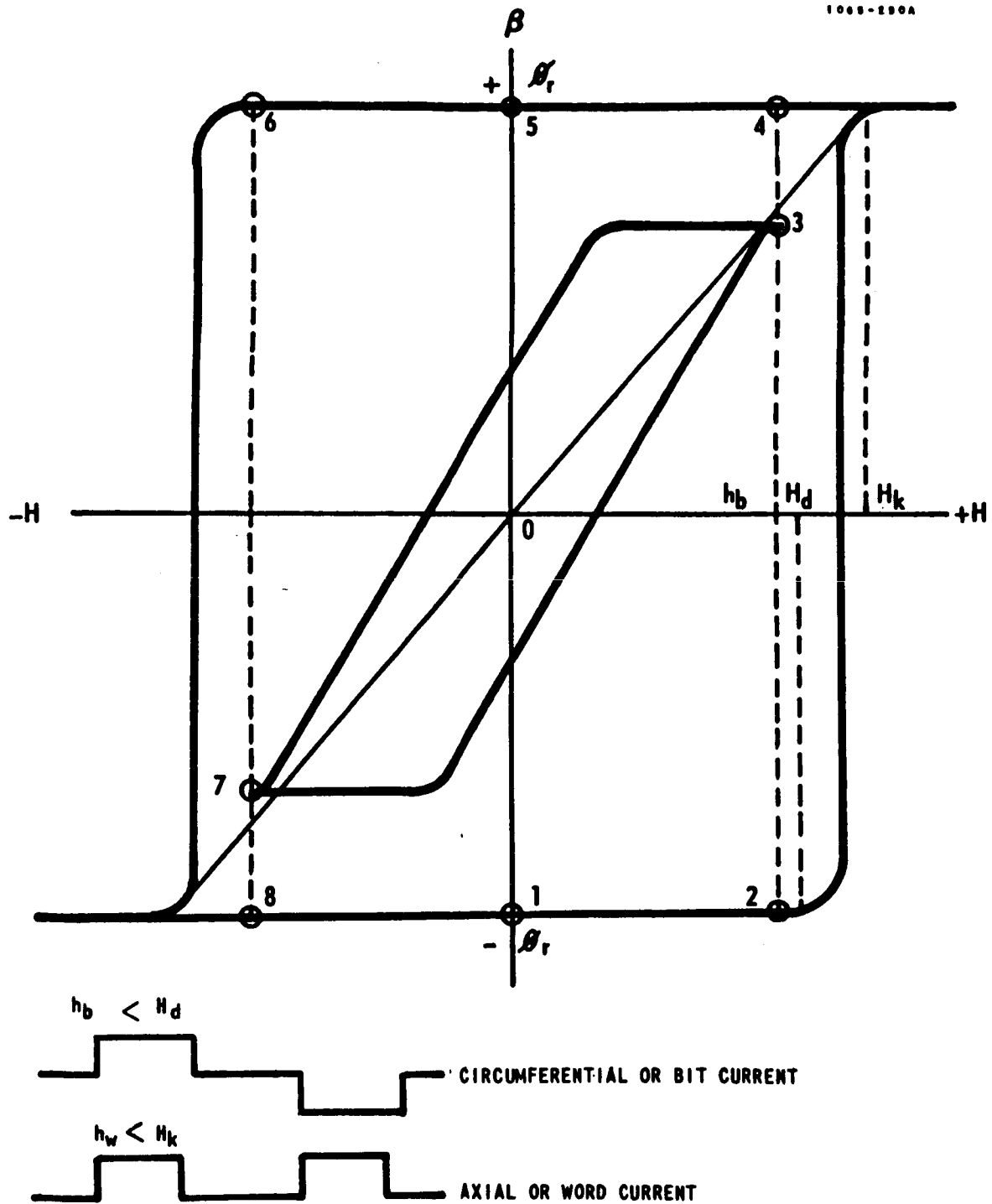
FIGURE 4. IDEAL MAGNETIZATION CURVES

Figure 5a shows the cross-section of a single MOS transistor. It consists of a block of N type silicon called the "body" or "substrate", into which P$^+$ impurities have been diffused in two parallel strips called, respectively, the "source" and the "drain". In operation, an induced P-region known as the "channel" connects source and drain. The surface of the silicon is covered by a protective layer of silicon dioxide formed during the silicon planar process and etched away along the longitudinal axes of the source and drain, exposing the silicon beneath. Metallic contacts are deposited over the exposed silicon area in the source and drain. The "gate" is a metallic conductor deposited over the oxide between the source and drain and separated from the source, drain, and substrate by the oxide.

If the gate, source, and substrate are grounded and a negative voltage is applied to the drain, no current will flow between source and drain since the drain-to-body P-N junction is reverse-biased. As a result, the source and drain are isolated from each other. However, if a negative voltage is also applied to the gate, electrons are repelled from the surface region of the silicon immediately beneath the gate and holes are attracted to it. As the gate-to-source voltage, V_{GS}, becomes more negative, this surface region finally changes or "inverts", becoming P-type instead of N-type. This inverted region, called the "channel", provides a path for conduction of the charge carriers between the source and drain so that, if the drain voltage is made appreciably more negative than the source, current flows from source to drain. Before the surface can be inverted to form a channel, the gate voltage must reach a certain threshold value V_T sufficient to neutralize surface charges. Typical processing can achieve a V_T of approximately -5V. Turn-on characteristics of a typical MOS FET are shown in Figure 5b.

As the gate voltage V_{GS} becomes more negative than V_T, the channel depth-- and hence conduction-- increases. For low currents, the channel behaves like a normal ohmic resistance, and the device operates in the linear region of its characteristic curve (Figure 5c), where the drain-to-source current I_{DS} is proportional to the drain-to-source voltage V_{DS}. As V_{DS} becomes more negative, however, the current eventually levels off or "saturates". The magnitude of current flow is now relatively independent of the drain-to-source voltage.

Depletion mode MOSTs operate in a similar manner except for the condition of zero gate voltage. Under this condition, the depletion mode MOST is turned on and conducts a finite value of drain current. This is due to the method of fabrication; a channel is formed in the device during
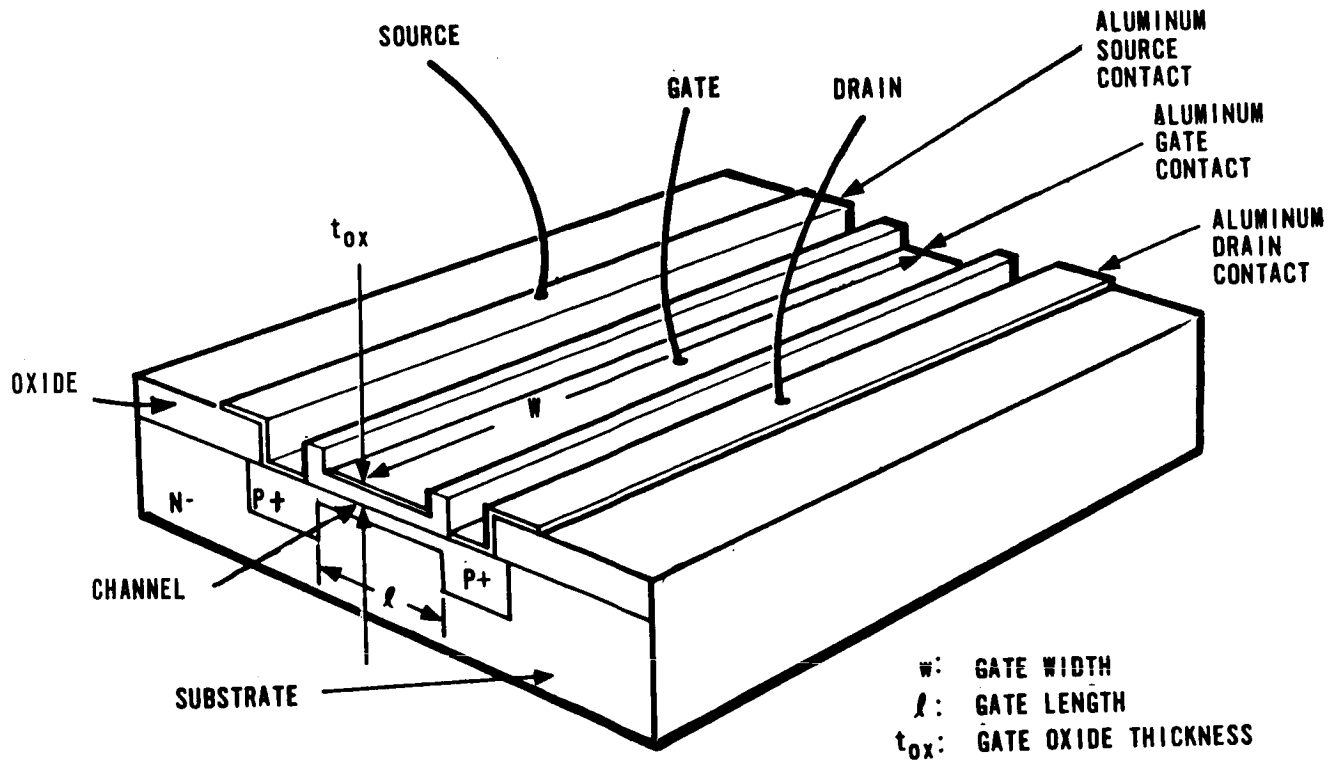
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w: GATE WIDTH
ℓ: GATE LENGTH
t_{ox}: GATE OXIDE THICKNESS

(a)

TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)

(b)
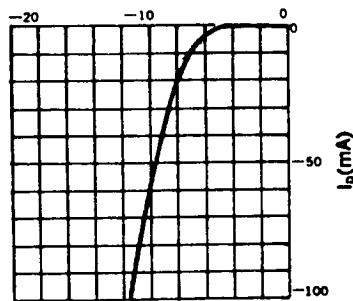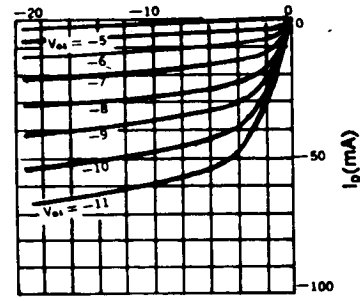
(c)

FIGURE 5. CROSS-SECTION OF MOS TRANSISTOR
AND ASSOCIATED CHARACTERISTIC CURVES

the manufacturing process. It becomes necessary to reverse bias the gate in order to reduce the drain current to zero. This reverse bias causes the cross-sectional area of the channel to be reduced to zero; hence the source and drain regions become back-to-back diodes and only diode leakage current is present. The depletion mode device has certain characteristics which make it more useful as an amplifier.

The more detailed characteristics of both the enhancement mode and the depletion mode MOSTs are discussed in other sections of this report.

4.0 SUMMARY

A comparison of address selection methods using MOS transistors was made. The interconnections were minimum where individual word drivers were used for each line. The complete selection circuitry and the associated word drivers are located on the same memory plane as the word lines, hence reducing the stack interconnections considerably.

The circuitry interfacing with the plated wire elements was investigated extensively. This consisted of the word driver and sense amplifier circuits. The limitations of the MOS transistor as a high current switching device were analyzed in terms of its geometry and operating parameters. Data were presented to demonstrate that the projected improvement in geometry and processing of the MOS transistor could enable it to be used effectively as a word driver for a plated wire memory element.

The detailed analysis of an all-MOST differential amplifier was performed to determine its limitations as a memory sense amplifier. The common mode rejection capability, utilizing present devices, does not appear to be sufficient for large common mode voltages, although the future fabrication of devices with better control of g_m and r_d will certainly show considerable improvement.

Both the word driver and the sense amplifier functions can be accomplished with MOS devices as will be demonstrated by the feasibility memory to be fabricated during the next phase of the contract.

The reduction of interfaces within a monolithic MOST logic function was investigated. Interconnections and crossovers are accomplished by the

utilization of common diffused regions, diffused "tunnels", and multilayer conductors. Materials and techniques for performing the interconnection and insulation of conductors was investigated also. An additional reduction of interconnection interfaces can be accomplished by the utilization of monometallic interconnection systems. The two most promising approaches appear to be either an all aluminum system or an all gold system. Interface interconnections are further reduced by the utilization of the interconnection concepts developed under a separate contract for use in the MICPAK packaging technique.

The complete selection circuitry for 16 word drivers was designed and a possible chip layout configuration investigated. The selection circuit consists of a four-stage F/F address register, decoding logic, word drivers, and clock circuits.

The fabrication processes of single type MOSTs, and combinations of MOSTs and bipolar transistors were investigated. The major process steps are outlined within the text of this report. As the number of types of devices increases, the complexity of the fabrication processes also increases. The plated wire manufacturing process is discussed briefly, showing the nonexistence of any manufacturing incompatibilities between MOS Devices and plated wires.

The advantages of complementary MOST logic circuitry were investigated. The major advantages over single type MOSTs are a significant increase in operating speed and a considerable reduction in power dissipation.

The cycle time of a 1,000-word plated wire memory utilizing P channel logic and N channel amplifier MOSTs was calculated to be 2.5 microsecond with a power dissipation of approximately 45 watts.

A breadboard NDRO memory system was fabricated with 16 words of two bits each. The electronics was constructed of all MOS transistors and consisted of the address register, decoding logic, word drivers, sense amplifiers, data register, and timing and control. The memory operated at a clock rate of 100 kc.

5.0 PACKAGE COMPATIBILITY BETWEEN THE MEMORY AND THE MOS DEVICES

The plated wire memory elements and the MOS functional blocks are physically smaller than ferrite toroids and discrete transistors hence, they can be very compatible when contained in the same package. During the course of the study phase of this contract, no aspects of the overall package revealed any incompatibilities between the memory and the MOS devices. The memory organization and package configuration is discussed in more detail in the following paragraphs.

Several approaches to the memory organization were discussed in the third monthly report. The most efficient organization is shown in Figure 6. A 512-word 28-bit (26 active and 2 spares) is used for illustration. The nine address bits from the processor are broken into two groups. The five lower bits are used for word selection in each of the 16 selection circuits. The remaining four bits are decoded and used to select the individual selection circuit. Each selection circuit module contains a five-bit storage register, a decoding tree, and 32 word driver MOSTs. Each word line has its own word driver device instead of the normal selection diode. Each complete plane contains 128 memory words and all the associated selection circuitry. There is one multilayer board for each stack which contains the timing and control, module select, sense amplifiers, bit drivers, and any necessary buffer circuitry required between the memory and processor.

The size of the memory stack is dictated by the following parameters:

1. Sense wire spacing

2. Word line size and spacing

3. Sense line replaceability

4. Memory word expansion

5. External interface requirements

6. Grounding requirements.

The solution to the optimization of these parameters led to the design of a multilayer memory plane on each side of two multilayer substrate boards as in Figure 7. The substrate boards are hinged on the frame to provide direct accessibility to the MOS functional blocks and sense wires.
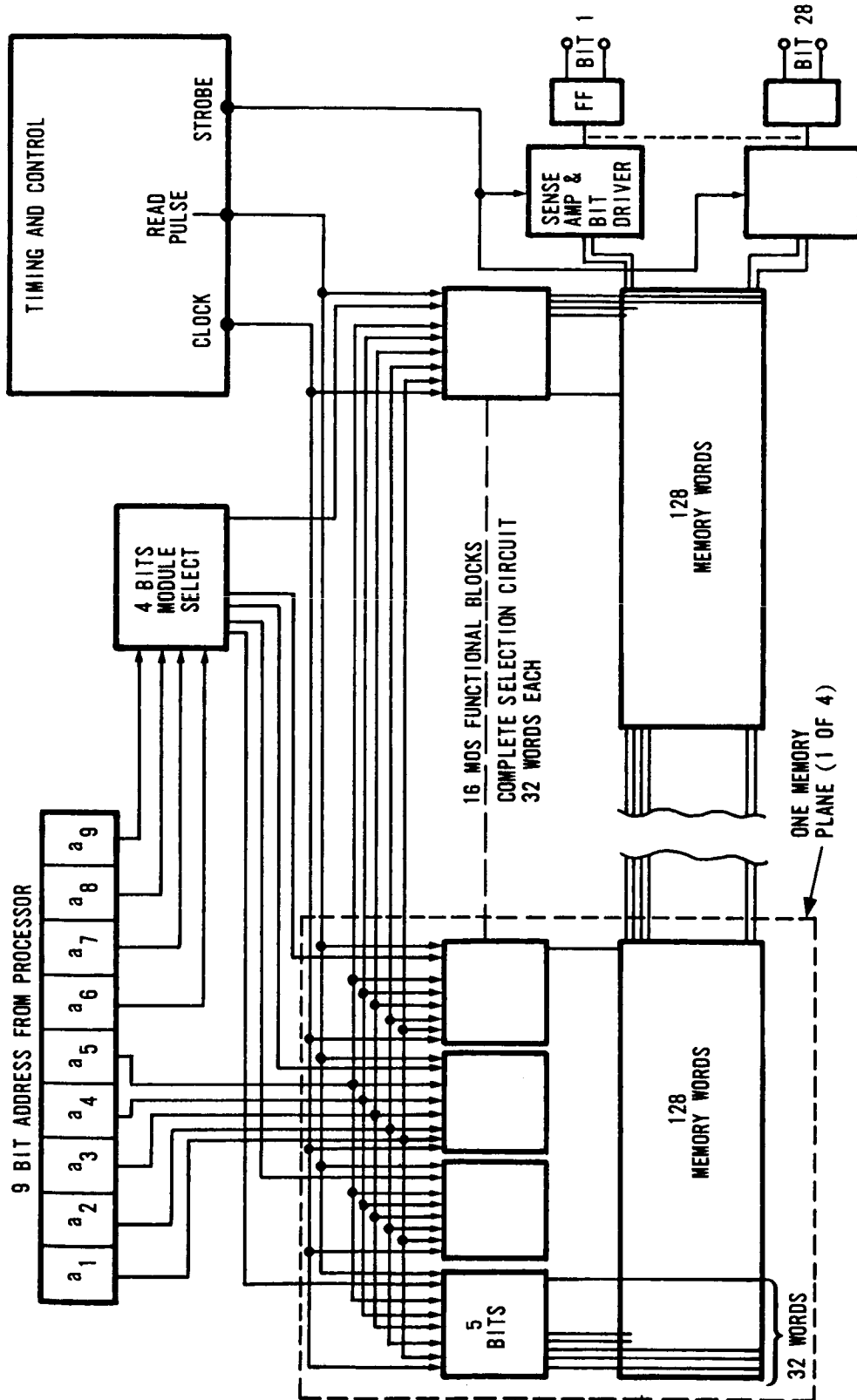
FIGURE 6. MOS PLATED WIRE MEMORY - 512 WORDS 26 BITS EACH

TOP COVER – REMOVED FOR STACKING

RECESSED BOTTOM COVER

EXTERNAL WORD SELECTION CONNECTOR

10.00

128 WORD PLANE TYPICAL OF 4

MOUNTING FRAME

5.50

1.5

SENSE LOOP CONNECTOR
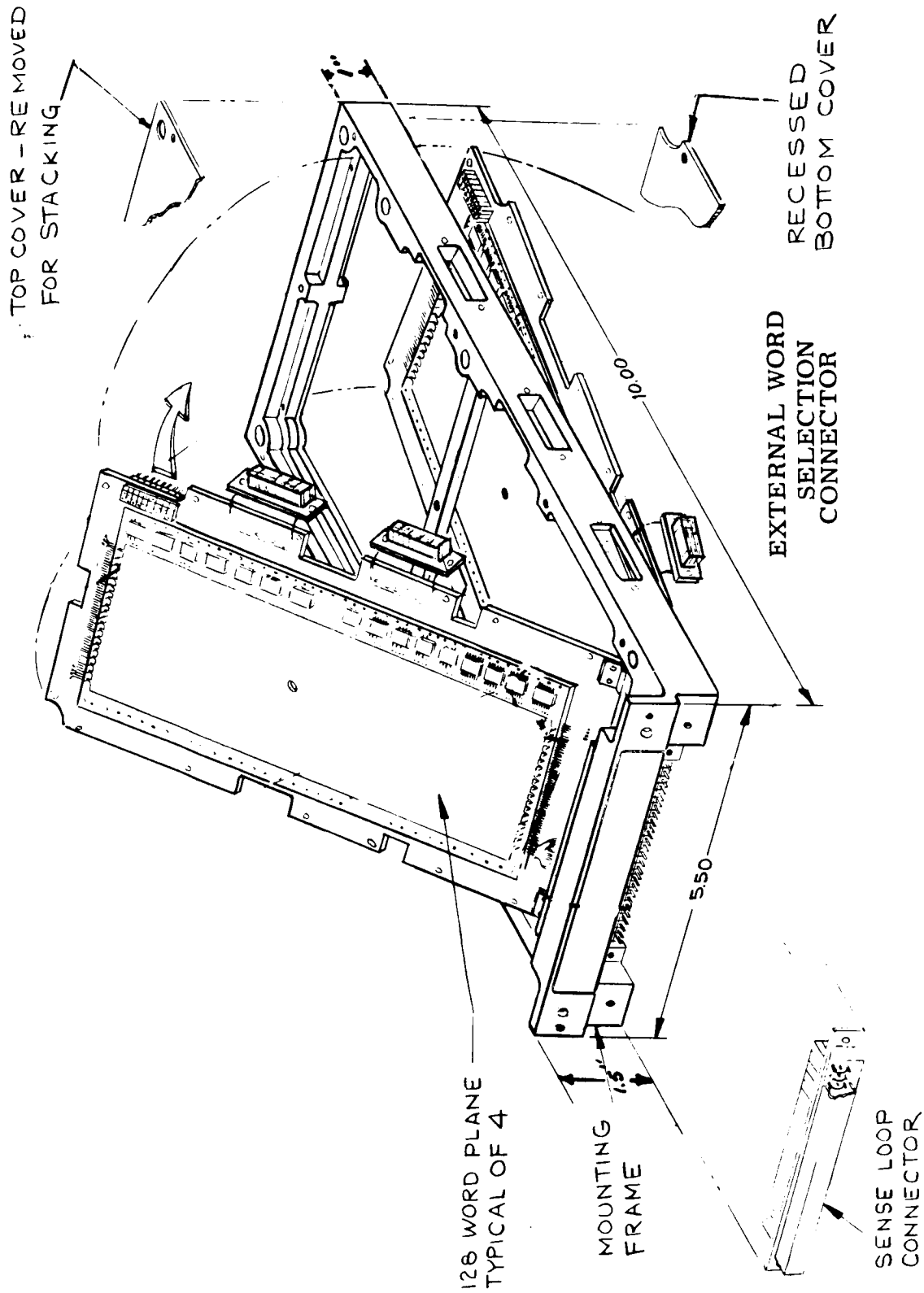
FIGURE 7. MEMORY STACK CONSTRUCTION

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6.0 INTERCONNECTIONS OF MEMORY TO MOS DEVICES

The interconnection of the memory and the MOS devices involves both electrical and mechanical interfaces.

The two major areas of electrical interfacing is the Word Driver and the Sense Amplifier. The MOS word driver circuit has the responsibility of generating current pulses of relatively large magnitude (200 to 400 ma) and with fast rise times (typically 50 nanoseconds). The MOS sense amplifier has the responsibility of detecting a very small signal (typically 5 millivolts) which occurs simultaneously with noise in the range of 50 to 200 millivolts and amplifying it to the voltage level required of the logic circuitry. These two functions can be accomplished with MOS transistors as will be shown in this section of the report.

The mechanical interface involves the reduction of interconnections and the reduction of the intermetallic interfaces present in the remaining interconnections. These are discussed in Sections 7 and 8.

6.1 MOS WORD DRIVER

The limitations of the MOS transistor as a high current switching device can be analyzed in terms of its geometry and its operating parameters.

Any device used as a word driver must be capable of supplying a pulse of 200 to 400 ma of current with a rise time or fall time of 50 nanoseconds, since the readout of an NDRO plated wire memory element occurs during both the rise and fall time of the word current pulse. The output can be sampled at either time. The magnitude of the output is a direct function of rise time or fall time which is about 50 nanoseconds for a reasonable output. The word driver device considered during this phase of the program is an enhancement type P channel MOS transistor.

The MOS transistor parameters which have the greatest effect on the word driver performance are as follows:

- Drain current: I_D

- Input capacitance: C_i

- Drain-to-Source "On" resistance: R_{on}

- Power dissipation

- Device Size (area)

- Breakdown voltages.

The drain current must be of the magnitude of 200 to 400 ma to drive a plated wire memory element. It is desirable to keep the input capacitance as low as possible in order to obtain the fastest possible rise or fall time of the gate-to-source input voltage. The drain "On" resistance contributes to the $I^2 R$ losses, current regulator requirements, and switching speeds. The maximum operating voltages are limited by device breakdown voltages. The device size and power dissipation dictates how many of these devices can be contained in a single integrated circuit chip.

Drain Current

The equation for the drain current capability of a MOS transistor is given by Sah [2] as:

$$I_D = \frac{\mu_p C_G}{L^2} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ in amperes} \qquad (1)$$

where:

μ_p is the surface mobility of holes in cm^2/volt-second.

C_G is the gate to channel capacitance in farads.

L is the gate length (separation of drain and source) in cm.

V_{GS} is the input gate-to-source voltage in volts.

V_T is the turn-on threshold of an enhancement type MOS transistor in volts.

V_{DS} is the drain-to-source voltage in volts.

The gate capacitance, C_G is the parallel plate capacitance of the gate electrode and the channel and is given as:

$$C_G = 0.08842 \frac{\epsilon_r L W}{t_{ox}} \text{ pf} \qquad (2)$$

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where:

ϵ_r is the relative dielectric constant of the oxide

L is the gate length: cm

W is the gate width: cm

t_{ox} is the oxide thickness: cm

Substituting for C_G, Equation 1 becomes:

$$I_D = 0.08842 \times 10^{-12} \frac{\mu_p \epsilon_r W}{L\, t_{ox}} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{amperes} \quad (3)$$

The properties μ_p, ϵ_r, t_{ox}, and L are limited by the materials and processing techniques used in manufacturing the MOS transistors. Surface mobility, μ, is a function of the conditions existing at the silicon surface and within the gate oxide, which are very hard to predict and control. (3, 4, 5, 6)

The cited references (2 through 6) indicate that the surface mobility of holes can vary from 94 to 204 $\frac{cm^2}{volt\text{-}sec}$ and the surface mobility of electrons can vary from 200 to 500 $\frac{cm^2}{volt\text{-}sec}$. Therefore, an N channel MOS transistor with similar geometry should be able to handle approximately twice the drain current.

The dielectric constant of the gate insulator is fixed as a result of the use of silicon dioxide which has a dielectric constant of approximately 4.0. Present processes use an oxide thickness, t_{ox}, of approximately 1000 Å, in order to obtain theoretical breakdown voltages up to 100 volts. The finished oxide surface is highly irregular, with many small areas which are considerably less than the desired 1000 Å thickness. These are the areas that limit the maximum usable gate voltage. This will also allow an increase in device drain current.

The gate length, L, of available devices is nominally 5 microns. This is an optimum value in keeping with present photolithographic techniques. Without pushing the state of the art gate lengths of 3 microns can be produced, and future processes should reduce this to 2 microns.

The gate-to-source threshold voltage, V_T, is not an inherent property of the basic material from which the MOS transistor is constructed, as is the case of the bipolar transistor. The bipolar base emitter threshold voltage is a function of the semiconductor material and doping. The MOS transistor threshold voltage is a function of the conditions existing at the semiconductor surface and within the gate oxide. Since these conditions are more a result of processing than material properties, the threshold voltage varies considerably from device to device [7]. (A typical MOS transistor will have a value of V_T equal to 5 volts with a ±1.0 to ±1.5-volt tolerance.) Therefore, the gate width, W, is by far the most practical method used today to control the final current handling capability of the MOS transistor.

The terminal characteristics of the optimum P channel word driver MOS transistor are:

 Drain to source voltage: -25 Vdc

 Gate to source voltage: -25 Vdc

 Gate to drain voltage: -25 Vdc

 Gate to source threshold voltage: -5 Vdc

 Gate to source capacitance: 8 pf

 Gate to drain capacitance: 5 pf

 Drain to source capacitance: 5 pf

 Drain to source "on" resistance: 12 ohms

This dictates a device with the following approximate geometrical dimensions:

 L_{GC} = Length of channel = 2.0 microns

 L_{SO} = L_{DO} = Length of entire overlap of gate metalization over source region = 2.0 microns

 T_{GOX} = Thickness of gate oxide = 750 Å

 W_G = Width of gate (channel = 180 mils)

 Chip size: 15 mils x 15 mils

A presently available P-channel MOS transistor capable of handling a maximum of 250 ma dc was examined in order to become more familiar with the device geometry necessary to handle this magnitude of drain current. (This device can handle current pulses in excess of 400 ma with power dissipation being the limiting factor.)

The General Instrument Corp. MEM517A was chosen for this purpose. The most important features of this device, other than the large value of drain current are:

- Drain to source voltage: -30 Vdc

- Gate to source voltage: -25 Vdc

- Gate to drain voltage: -25 Vdc

- Gate to source capacitance: 16 pf

- Gate to drain capacitance: 10 pf

- Drain to source capacitance: 10 pf

- Drain to source "on" resistance: 30 ohms

- Gate length: 0.45 mil

- Gate width: 180 mils

- Chip size: 45 mils x 45 mils

Input Capacitance. The input capacitance of a MOS transistor, together with the driving source impedance determine, to a great extent, the maximum switching speed of the drain current.

As discussed in the previous paragraphs, a MOS transistor capable of handling the required word current will have a very wide gate region which results in a large value of input capacitance (15 to 25 pf). The input capacitance consists of the active gate capacitance, the drain and source overlap capacitances, and the stray capacitance associated with the gate metalization which extends out over the body where external contact to the chip is made.

The sum of these capacitances is given as:

$$C_i = C_G + C_{GS} + (A-1) C_{GD} + C_{GB} \qquad (4)$$

where:

C_i = total input capacitance

C_G = active gate capacitance (between gate and channel)

C_{GS} = capacitance between the source and that part of the gate electrode which overlaps the source region.

C_{GD} = Capacitance between the drain and that part of the gate electrode which overlaps the drain region.

$(A-1)C_{GD}$ = Miller feedback capacitance

C_{GB} = capacitance between that part of the gate electrode which extends out over the silicon body (substrate) and provides the bonding area for the external connection.

The locations of these capacitive elements within the silicon chip are shown in Figure 8. The input capacitance measures approximately 25 pf which is approximately equal to C_i of Equation 4, including the Miller effect. In current mode applications such as the word driver, the voltage gain is normally very low, hence the Miller effect becomes negligible. A MEM517A was cross-sectioned to determine its geometrical dimensions. A schematic diagram of the device cross-section is shown in Figure 9. The dimension designations and the measured values are:

L_{GM} = Length of gate metalization = 12.5 micron = 9.5 mils

L_{OX} = Length of gate oxide = 7.5 microns = 0.3 mil

L_{GC} = Length of channel = 3.5 microns = 0.14 mil

L_{SG1} = L_{DG1} = Length of lateral diffusion of source and drain respectively under gate oxide = 2 microns = 0.08 mil

L_{SG2} = L_{DG2} = Length of overlap of gate metalization over source oxide and drain oxide respectively = 2.5 micron = 0.1 mil

$L_{SO} = L_{DO} =$ Length of entire overlap of gate metalization over source and drain regions respectively ($L_{SG1} + L_{SG2}$ and $L_{DG1} + L_{DG2}$) = 4.5 microns = 0.18 mil.

$T_{GOX} =$ Thickness of gate oxide = 1000 $\overset{\circ}{A}$ = 0.004 mil

$T_{SOX} =$ Thickness of source oxide = 1000 $\overset{\circ}{A}$ = 0.004 mil

$T_{DOX} =$ Thickness of drain oxide = 1000 $\overset{\circ}{A}$ = 0.004 mil

From these measurements, the capacitive elements were calculated and are:

$C_{GC} =$ Gate to channel capacitance = 5.7 pf

$C_{GS} =$ Gate to source overlap capacitance = 7.2 pf

$C_{GD} =$ Gate to drain overlap capacitance = 7.2 pf

$C_{in} = C_{GC} + C_{GS} + C_{GD} =$ 20.1 pf

This value of C_{in} does not include the capacitance contributed by the gate protection zener. Taking the zener capacitance into consideration, the total input capacitance compares favorably with the measured value (25.5 pf). Since drain current is a function of gate to channel capacitance, C_{GC}, only a small part of the total input capacitance contributes to drain current. The remaining capacitances are parasitic and degrading to circuit performance and should be minimized as much as practical. Tolerances associated with present day photolithographic techniques result in the large values of overlap capacitances. Future improvements should reduce this considerably.

The rise and fall times of the word driver drain current are a direct function of the input capacitance C_i and the driving source impedance. MOS transistors normally have negligible storage and delay times, therefore the drain current follows the voltage applied to the gate electrode. Since the driving source impedance is normally much greater than the values of r_D, r_S, and r_C, the equivalent circuit shown in Figure 10 can be reduced to a lumped capacitance C_i, as expressed by Equation 4. The composite equivalent circuit of the driving source and the MOS transistor can be represented by a simple RC network as shown

in Figure 11. Once the word driver device characteristics have been defined, the input capacitance becomes fixed. The maximum allowable driving source impedance can now be determined. For example, to obtain a word current rise and/or fall time on the order of 50 nanosec with a single MEM517A requires a driving source impedance of:

$$R_{gen} = \frac{50 \text{ nsec}}{4 \ C_i}$$

$$= \frac{50 \times 10^{-9}}{4 \times 25 \times 10^{-12}} = 500 \text{ ohms}$$

This information can be used to define the geometry of the MOS transistor which drives the word driver device.

Word Driver Test Circuit. A word driver circuit was implemented as shown in Figure 12. The circuit was used to drive an actual plated wire memory element. Information was stored on the wire by use of a dc writing technique where a current is passed through the plated wire in either of two directions. A "1" or "0" is stored as a result of the direction of current flow. The NDRO mode of reading was utilized and the resultant output voltage waveform and the word current is shown in Figure 13. The magnitude of I_w was 400 milliamps and was controlled by adjusting the supply voltage V_{DD2}. The output voltage was approximately 17 millivolts. The value can be expected to be reduced to 8 to 10 millivolts under normal stack operating conditions where the stored bit becomes disturbed and the output signal becomes attenuated. The large rise time of the word current (I_w) was a result of the RC time constant associated with the 2.0 k ohm resistor and the input capacitance of the MEM517As. Since the "on" resistance of the MEM520 is typically 250 ohms, the capacitance discharges very rapidly, and a 50 nanosecond fall time of the word current is obtained. It is during this fast fall time that the output of the plated wire is sensed. This circuit illustrates the duty cycle problem inherent when only P channel devices are used. In order to obtain the proper output voltage swing, the load resistor must be at least 10 times as large as the "on" resistance of the active MOS device. This results in a long RC time constant, hence a low duty cycle. The use of complementary (N channel and P channel) enhancement mode MOS transistors allows a more efficient circuit to be mechanized as illustrated in Figure 14. The on resistance of both MOSTs is on the order of 250 ohms, providing a short RC time constant during both turn-on and turn-off of the word current transistor. The word current pulse

and the output signal are shown in Figure 15. As can be seen the use of complementary MOSTs allows the memory to operate at a faster cycle time. The overall cycle time (including address and decoding logic) of a large memory may be reduced from about 8 to 10 microseconds to about 2 to 4 microseconds.

6.2 MOS SENSE AMPLIFIER

The requirements of a circuit to amplify the small, high frequency output of a plated wire memory stack into a usable logic level signal, can be summarized as follows: Each data signal is typically a few millivolts in amplitude and generally contains a fundamental of at least 20 MHz. The amplifier must be capable of rejecting large common mode signals both during and before signal time. The largest transient signal occurs prior to "read-time" as a result of a preceding "write" or "store" operation. Naturally, the circuit must recover from these input transients in order to accept the next data output signal. Since the operating output signals from a memory sense line cannot be predicted on a repetitive basis, the amplifier requirements are more of a quasi-transient nature.

A common, straightforward approach to the design of this circuit is a dc-coupled, differential amplifier. This approach minimizes the number of associated discrete components, thus resulting in minimum inter-connects and package size. Direct coupling the stages of the amplifier also improves the recovery characteristics of the circuit. This improvement is simply a result of the much lower inter-stage RC time constant. As usual, however, a trade-off between this advantage and the dc offset problem must be considered. Offset is a result of differences in the linear region characteristics of the individual stage devices, i.e., in the case of the FET's the quiescent levels of the drains are important. Naturally, the offset of one stage will affect the operating point of the following stage. In all direct coupled differential amplifiers this problem is minimized by matching devices; however, the remaining value is referred to the input in order to evaluate its significance in the application. The worst case memory stack output must be capable of overcoming the amplifier's input offset and provide enough signal to be amplified to the detector to the trigger level.

Typical Amplifier Specifications:

    Operating temperature range: -55°C to 125°C

    Voltage supply tolerance: ±5 percent

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Voltage gain: 6000 to 8000 volts/volt

Operating frequency range: 0 to 20 mHz

Common mode rejection ratio: 1000 : 1 (to 1V)

Common mode frequency range: 0 to 20 mHz

Minimum input voltage range: 1 to 10 mv

Offset (referred to input):   1 mv

The most difficult specification to meet, using MOS devices, is the common mode rejection ratio. To obtain common mode rejection, a balanced circuit such as a differential amplifier is required. In a differential amplifier the first stage must provide the common mode rejection since differential signals at the output of the first stage that are caused by common mode input signals are indistinguishable from differential outputs caused by differential inputs. Therefore, the common mode rejection ratio of a differential amplifier depends upon the symmetry of the first stage of the differential amplifier. For the circuit shown in Figure 16, it was shown in the 5th monthly report that the common mode rejection ratio is limited by

$$CMRR = (1 + \mu)\left(\frac{\mu}{\delta \mu}\right)$$

where μ is the average voltage gain, $\delta \mu$ is the deviation of μ from the average in each side. For a common mode rejection ratio of 1,000 the change in voltage gain must be less than

$$\frac{1 + \mu}{1,000}$$

$$\frac{\delta \mu}{\mu} = \frac{\delta r_d}{r_d} + \frac{\delta g_m}{g_m} \leq \frac{1 + \mu}{1,000}$$

The μ is usually less than 30 so that

$$\frac{\delta \mu}{\mu} = \frac{\delta r_d}{r_d} + \frac{\delta g_m}{g_m} < 0.03$$

Obtaining a three percent match in voltage gain is unrealistic at the present time especially with an integrated MOST circuit. Other unbalances in circuit parameters will also decrease the common mode rejection ratio so that a slightly tighter specification on μ would be required in an actual circuit.

Another factor which affects the design is the bandwidth. For an MOS transistor the maximum bandwidth is approximately.

$$f = \frac{1}{2\pi R_L \left[C_{ds} + C_{dg} + C_i \right]}$$

where C_{ds} is the drain to source capacitance, C_{dg} is the drain to gate capacitance, C_i is the input capacitance to the next stage, and R_L is the load resistor. The approximate gain that can be obtained with one stage is:

$$G = g_m R_L$$

The gain bandwidth product is

$$GBW = Gf = \frac{g_m}{2\pi \left[C_{ds} + C_{dg} + C_i \right]}$$

Using typical values for C_{dg}, C_{ds}, and C_i of 0.5, 1.5 and 6 pf's respectively gives

$$GBW = (g_m) (2) 10^{10}$$

For a bandwidth of 20 MHz

$$G = g_m \times 10^3$$

At the present time the transconductance is between 5 and 10 millimhos for the values of capacitance that were assumed. The gain per stage is between five and ten and $R_L \cong 1 \text{ K } \Omega$. Thus at least four stages are required, and probably five will be necessary, to meet the gain requirements.

The above considerations indicate that a differential amplifier meeting all the requirements listed is not feasible at the present time. Additional effort in reducing the variations in the MOST parameters could lead to a practical differential type sense amplifier.

An approach to a sense amplifier which appears to be more practical is shown in Figure 17. In this approach the desired common mode rejection ratio is obtained with balum transformers. Obtaining the common mode rejection in this way permits the use of a single-ended amplifier. To obtain a gain of 8000, five stages are needed. Several features of the single-ended amplifier are:

Biasing - an enhancement mode MOS transistor is easy to bias with a single drain to gate resistor.

Drift - MOS transistors are noted for high drift rates. Therefore, the dc gain must be much less than the ac gain. Two methods are available for reducing the dc gain: ac coupling, and dc feedback. AC coupling is shown in Figure 17 since dc feedback has the disadvantage of requiring the feedback path to have a very low cutoff frequency. The low frequency break would occur at about 100 Hz. DC feedback around each stage is an alternative method that could be used, but it would require more parts that are more difficult to integrate.

Strobing - a five stage sense amplifier would present problems in strobing since each sense amplifier may have a different time delay. The strobe pulse must arrive at the amplifier at the proper time to block the read noise and pass the signal.

Recovery - an ac coupled sense amplifier requires time to recover from large differential signals that occur during the "write" mode. The recovery time depends upon the coupling capacitors and the saturation impedance levels.

Assuming the gain and bandpass requirements could be met, the remaining general problem areas are in interstage coupling, frequency stability, and threshold drift. If the drift characteristics cannot be more closely controlled, the amplifier would necessarily need to be RC coupled. As previously mentioned, this coupling technique is undesirable where large input transients can be expected. With the use of a more stable gate insulation such as silicon nitride, the device's drift characteristics may be more closely controlled.

The gain-bandwidth (GBW) product may be increased by the optimization of the device geometry. The gain-bandwidth product is given as [8].

$$GBW = \frac{g_m}{2\pi C_T} \tag{7}$$

where:

for a single stage amplifier: $C_T = C_{DG} + C_{DS}$

for several cascaded stages: $C_T = C_{DG} + C_{DS} + C_{GS}$

It can be shown that the GBW product is inversely proportional to the gate length. By reducing the gate length by a factor of 2; g_m, and as a direct result, GBW will be increased by a factor of 2. Other factors which can be used to increase the GBW product are: N channel transistors have a carrier mobility factor at the surface which is greater than that of a P channel device by at least a factor of 2; gate-to-source overlap capacitance can be minimized by the use of more accurate photolithographic techniques; the gate-to-drain capacitance (which is the familiar Miller feedback capacitance) can be minimized by using a depletion mode device which has the gate electrode offset from the drain region; and drain to source junction capacitance can be minimized by the reduction of the drain surface area. The implementation of all these factors tend to indicate that the GBW of a multistage MOS transistor amplifier could be increased by a factor of 2 to 5. This should provide an N channel device with the following parameters:

Breakdown voltages: 30 Vdc minimum

g_m, transconductance: 12,000 μmhos

C_{DG}, drain to gate capacitance: 0.1 pf

C_{DS}, drain to source capacitance: 0.8 pf

C_{GS}, gate to source capacitance: 3.4 pf
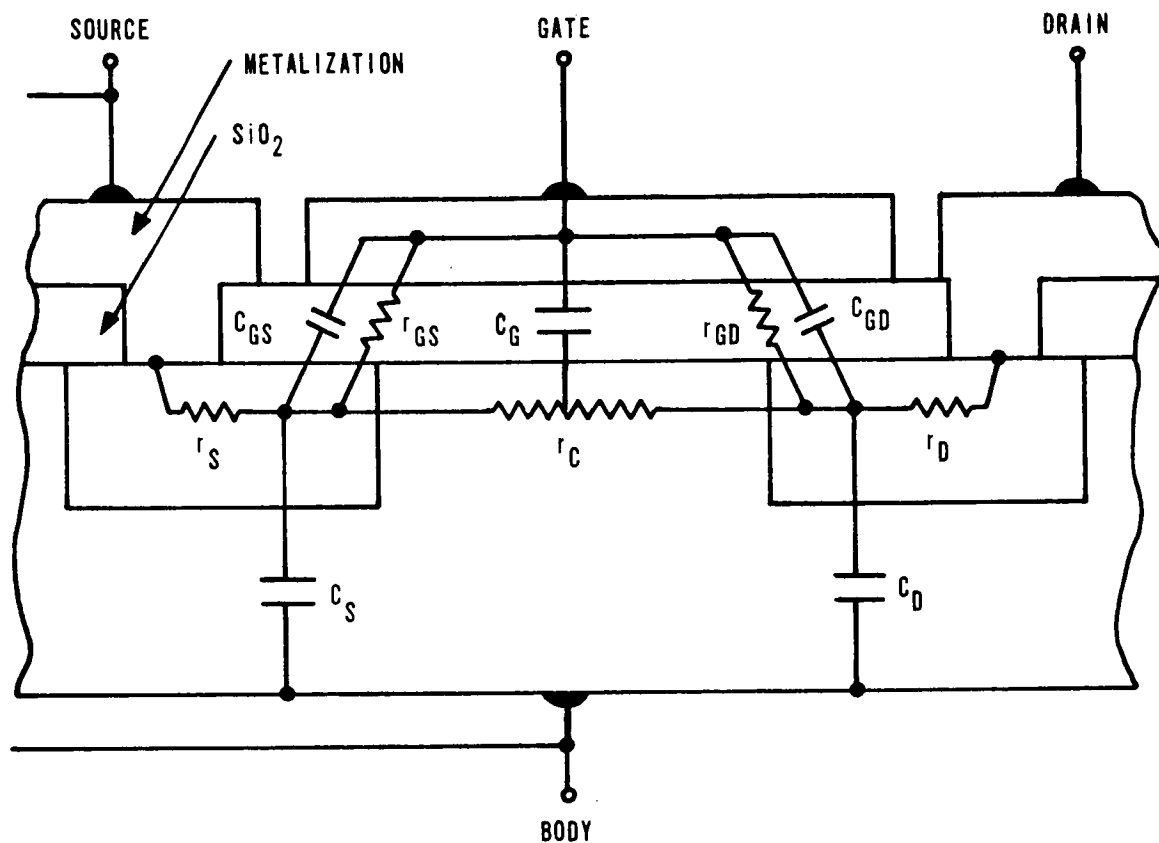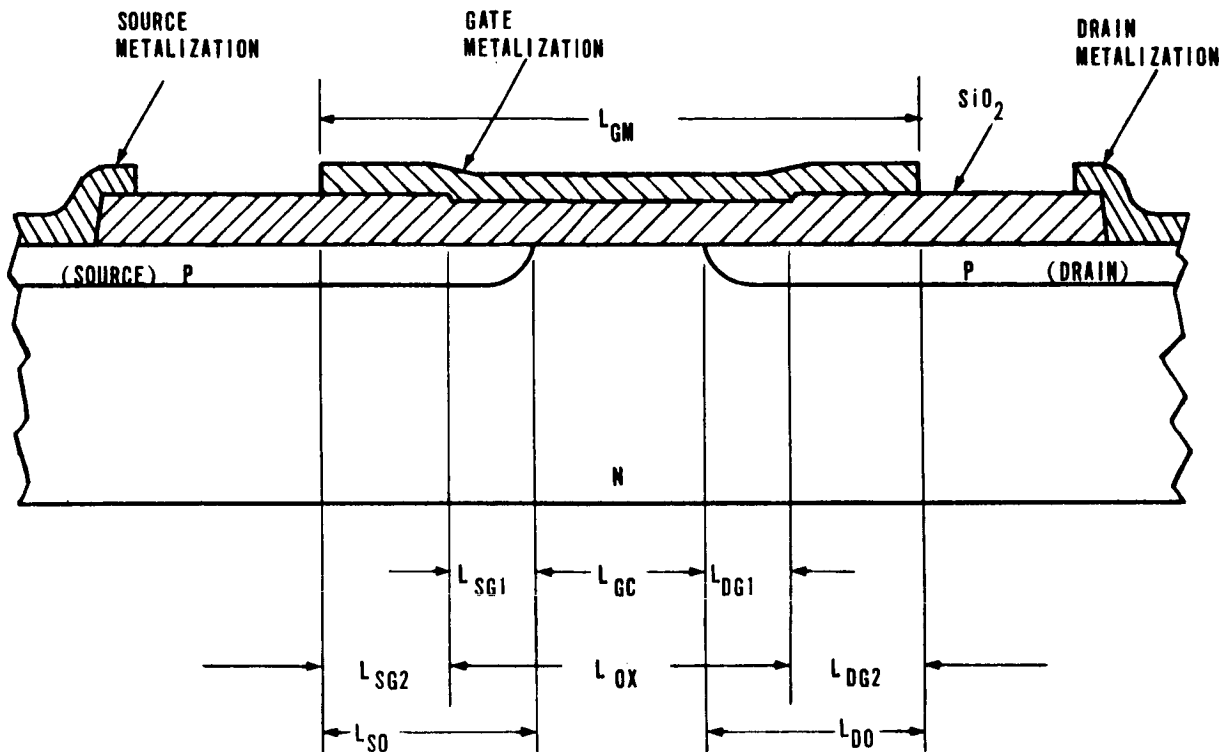
GBW, gain bandwidth product: 450 mc

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SOURCE   GATE   DRAIN

METALIZATION

SiO₂

C_{GS} r_{GS} C_G r_{GD} C_{GD}

r_S r_C r_D

C_S C_D

BODY

FIGURE 8.   CROSS-SECTIONAL SCHEMATIC DIAGRAM OF A
MOS TRANSISTOR CHIP SHOWING THE LOCATION
OF CAPACITIVE AND RESISTIVE ELEMENTS

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L_{GM} — LENGTH OF GATE METALIZATION.

L_{OX} — LENGTH OF GATE OXIDE.

L_{SG1} — LENGTH OF LATERAL DIFFUSION OF SOURCE UNDER GATE OXIDE.

L_{DG1} — LENGTH OF LATERAL DIFFUSION OF DRAIN UNDER GATE OXIDE.

L_{SG2} — LENGTH OF OVERLAP OF GATE METALIZATION OVER SOURCE OXIDE.

L_{DG2} — LENGTH OF OVERLAP OF GATE METALIZATION OVER DRAIN OXIDE.

L_{GC} — LENGTH OF CHANNEL.

L_{SO} — LENGTH OF ENTIRE OVERLAP OF GATE METALIZATION OVER SOURCE REGION

L_{DO} — LENGTH OF ENTIRE OVERLAP OF GATE METALIZATION OVER DRAIN REGION

FIGURE 9. CROSS-SECTIONAL SCHEMATIC DIAGRAM OF
GENERAL INSTRUMENT'S MEM517A SHOWING GATE
METALIZATION OVERLAP OF SOURCE AND DRAIN

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FIGURE 10. EQUIVALENT CIRCUIT OF A MOS TRANSISTOR
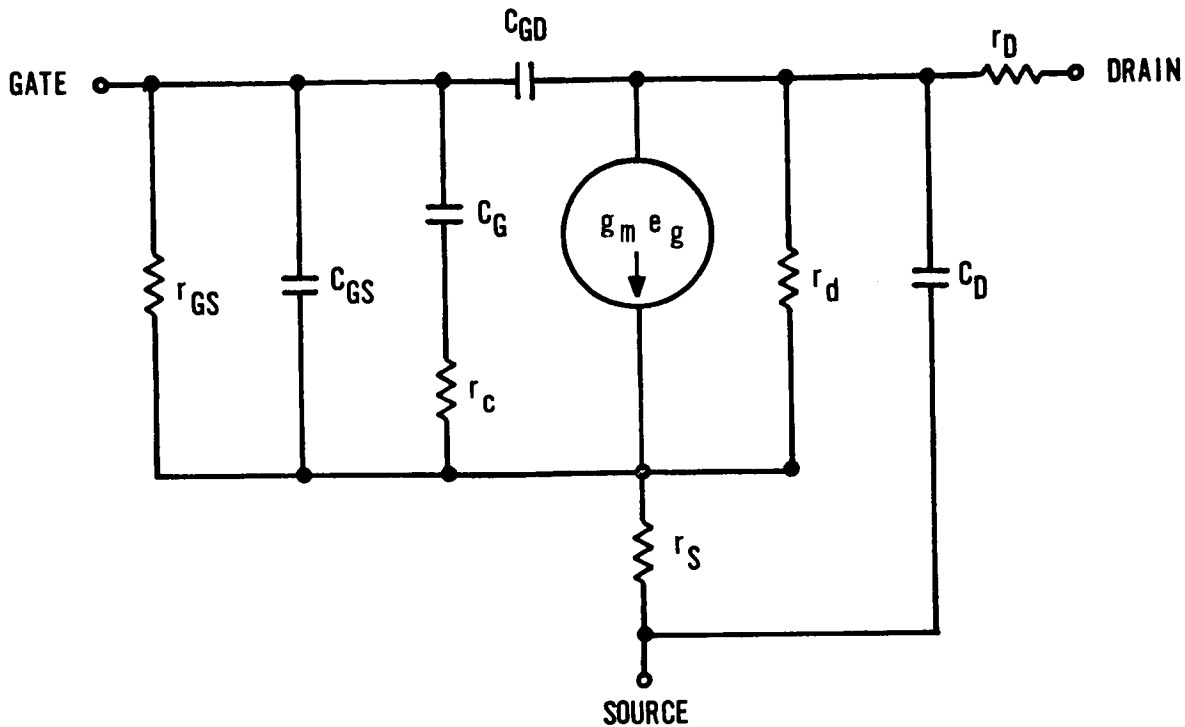
where: r_{GS} = Gate-to-Source oxide leakage resistance

C_{GS} = Gate-to-Source capacitance (includes the capacitance contributed by the extension of the gate contact region and over the body).

C_G = True Gate-to-Channel capacitance

r_c = Channel resistance

C_{GD} = Gate-to-Drain overlap capacitance

r_d = Dynamic drain resistance

r_S = Resistance of source region and ohmic contact

r_D = Resistance of drain region and ohmic contact

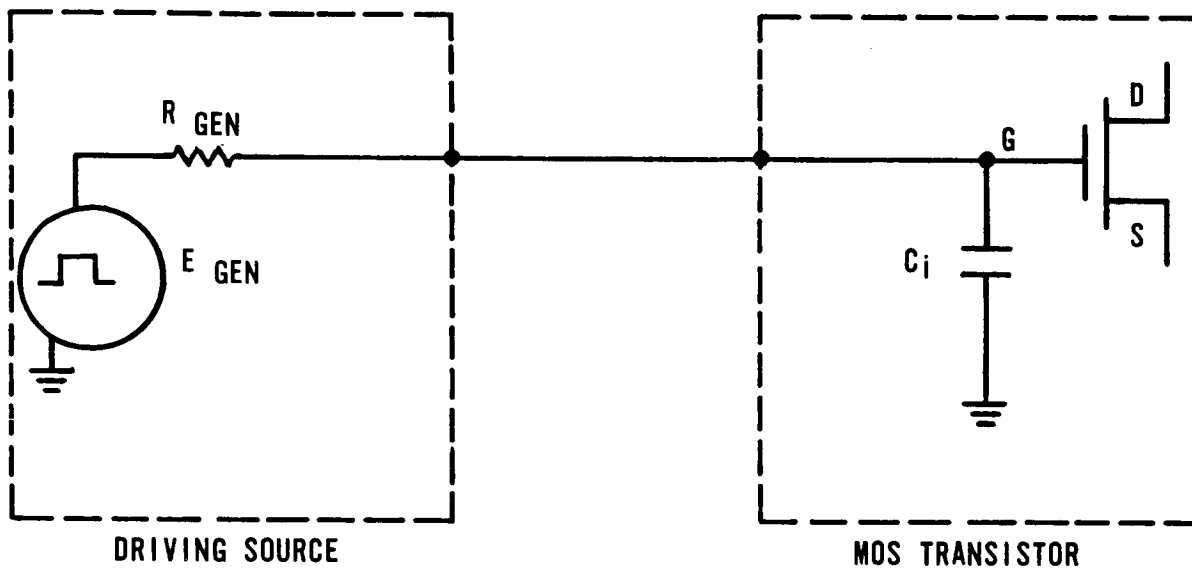C_D = Drain-to-Body (or source) capacitance

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FIGURE 11. COMPOSITIVE EQUIVALENT CIRCUIT OF A HIGH
CURRENT MOS TRANSISTOR AND ITS DRIVING SOURCE
IMPEDANCE USED TO DETERMINE OUTPUT
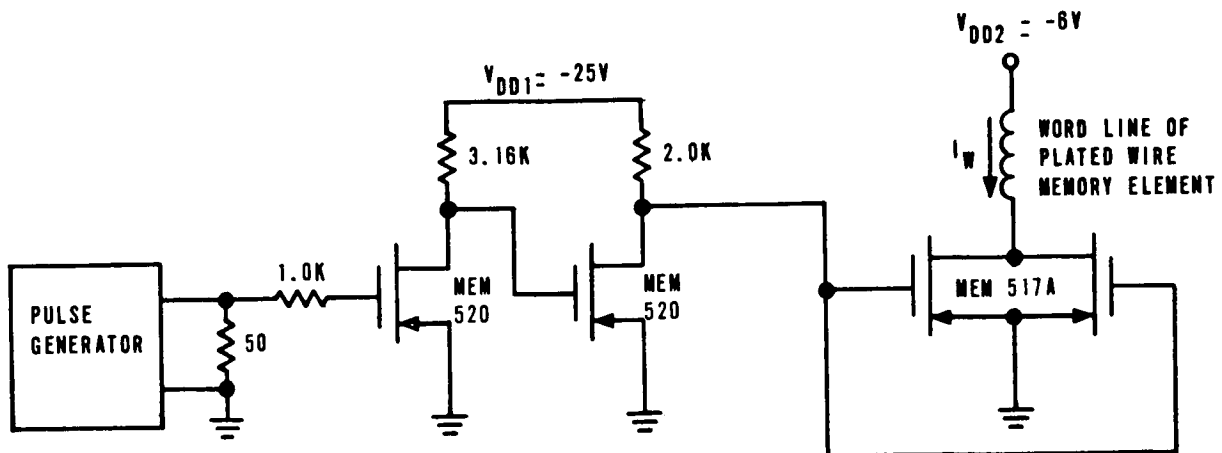CURRENT RISE AND FALL TIMES

0766-287A

FIGURE 12. SCHEMATIC DIAGRAM OF MOS TEST CIRCUIT USED
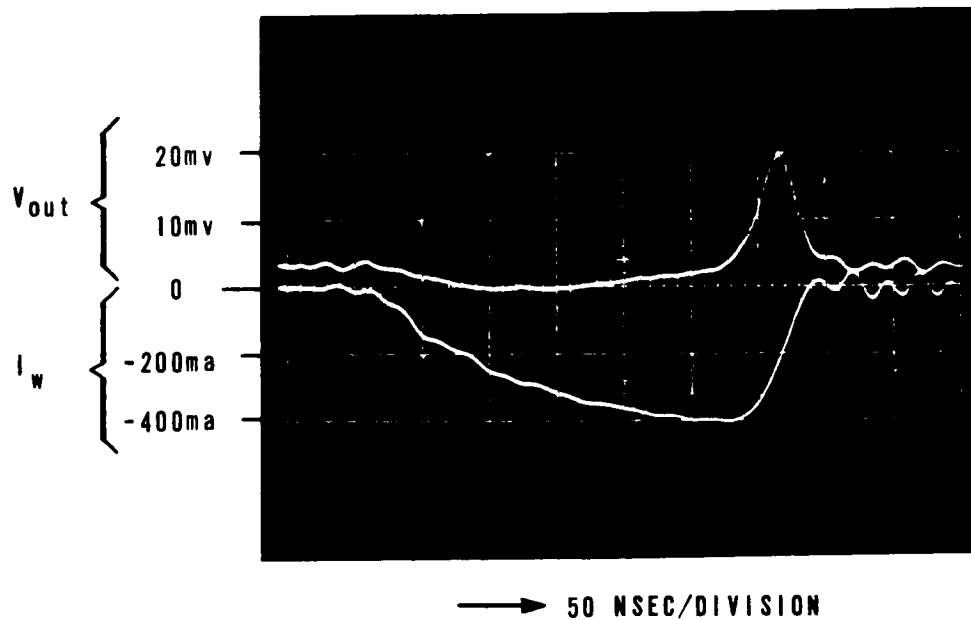TO DRIVE THE PLATED WIRE MEMORY ELEMENT

FIGURE 13. PHOTOGRAPH OF WORD CURRENT WAVEFORM AND
SENSE VOLTAGE WAVEFORM OBTAINED WITH THE
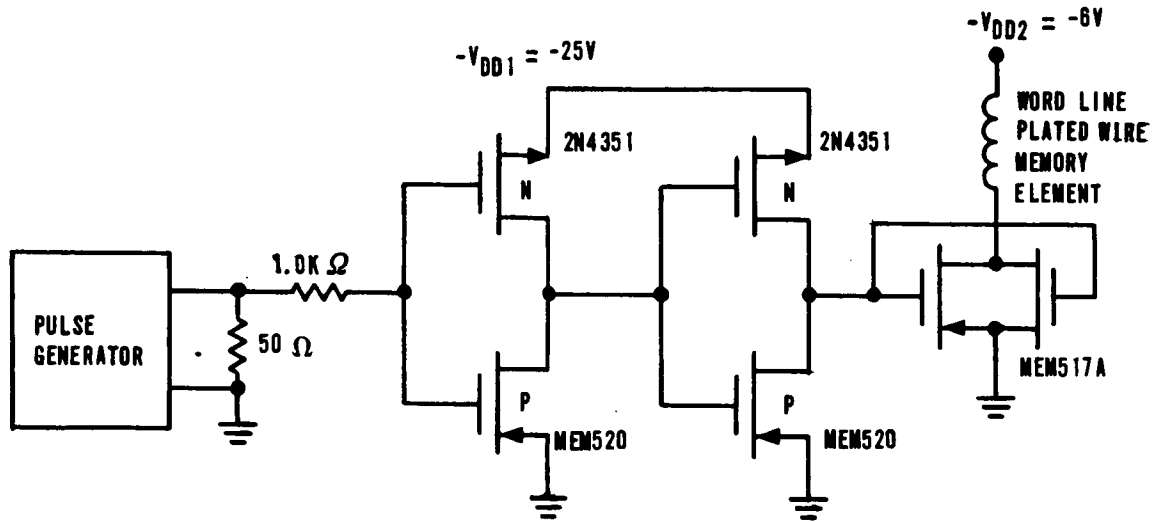ABOVE CIRCUIT

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FIGURE 14. SCHEMATIC DIAGRAM OF COMPLEMENTARY
MOS TRANSISTOR WORD DRIVER

50 NSEC/DIVISION
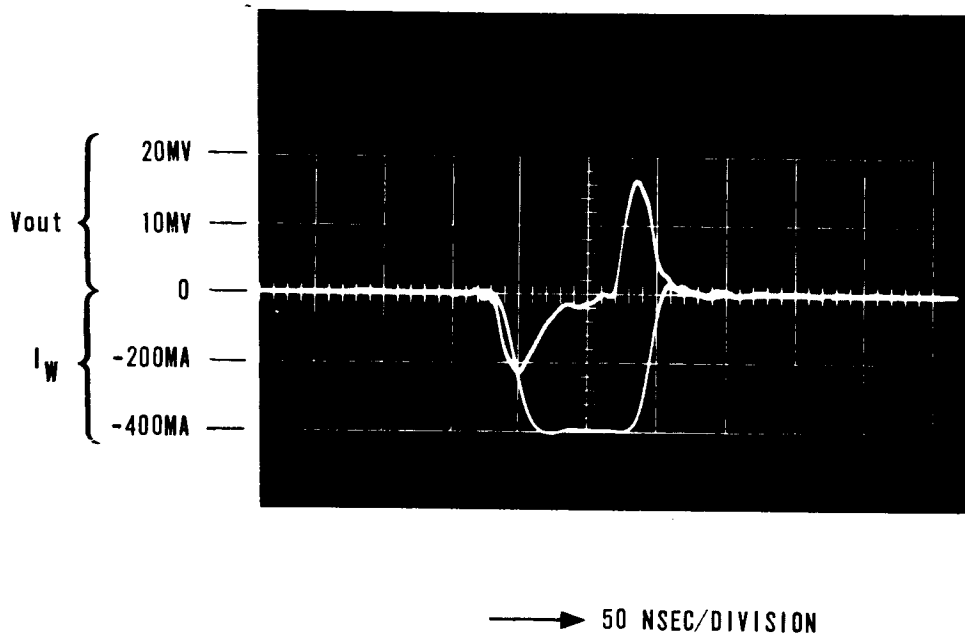
FIGURE 15. PHOTOGRAPH OF WORD CURRENT WAVEFORM
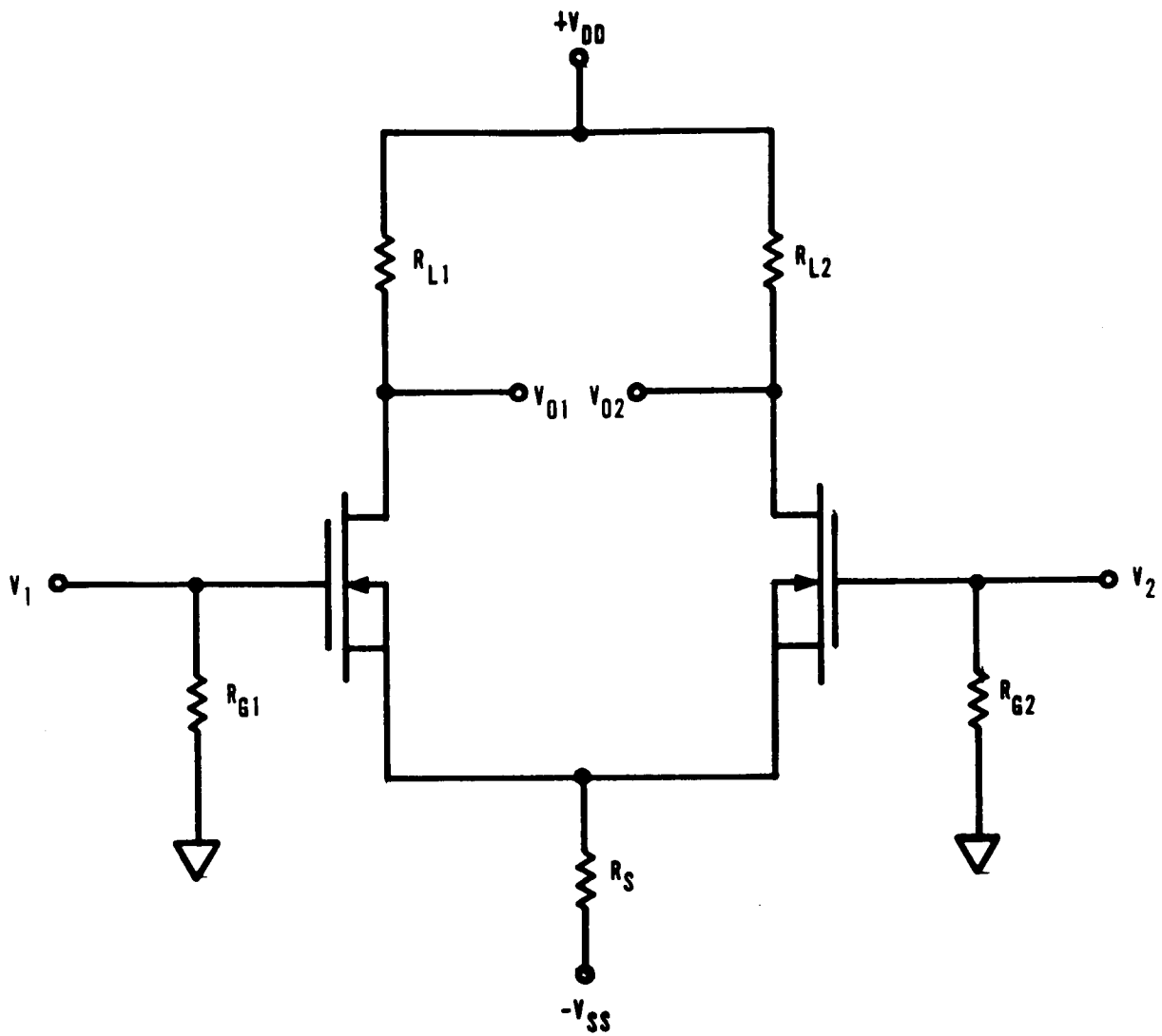AND SENSE VOLTAGE WAVEFORM OBTAINED
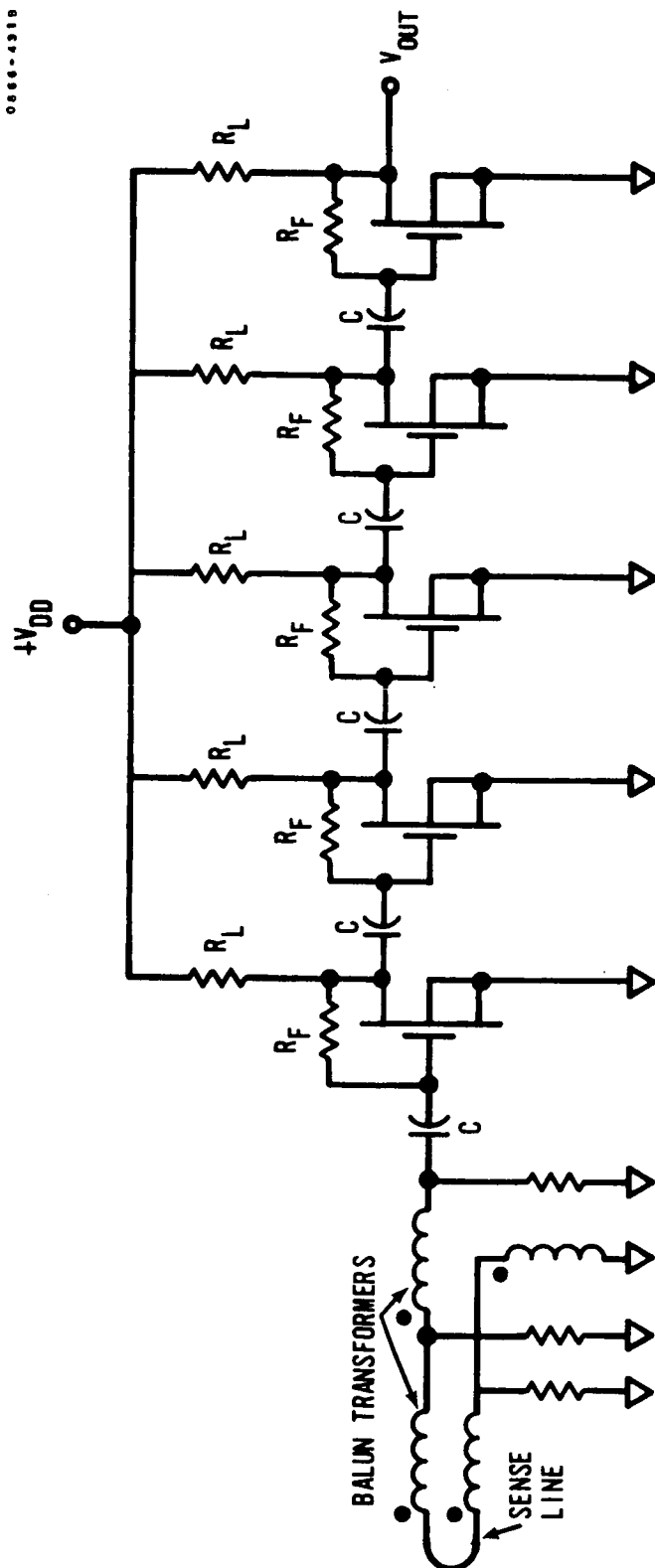WITH THE ABOVE CIRCUIT

FIGURE 16. MOST DIFFERENTIAL AMPLIFIER

FIGURE 17. AC COUPLED MOST SENSE AMPLIFIER

7.0 INTERCONNECTION OF MOST LSIs AND PLATED WIRE

Once the interconnection system has been solved at the LSI chip level, it becomes desirable to provide a compatible system of external interconnections so that circuit continuity is provided with a minimization of metallic interfaces. The LSI interconnection system is discussed in more detail in Section 8. The technique presently being developed is compatible with an all-aluminum interconnection system.

Honeywell has developed a technique for depositing aluminum on a polyimide, "H", film.* This development (partially funded by NADC and RADC development contracts) has proven the feasibility of using vapor-deposited aluminum conductors on a supporting polyimide film to perform this interconnection. Polyimide film is similar to Mylar in properties except it can withstand all process temperatures encountered in integrated circuit assembly. The application of this technique to the interconnection of integrated circuits is shown schematically in Figure 18. Briefly stated, the process is:

1. Evaporate the conductor onto the film.

2. Photoetch the desired interconnect pattern into the conductor metal in a manner analogous to making flexible printed circuits.

3. Bond the aluminum conductors on the film to the contact pads on the chip using thermo-compression or ultrasonic bonding.

4. Electrically test the chip/lead film assembly.

5. Package completed assembly.

6. Assemble the packaged circuits onto the anodized printed wiring board (PWB) and attach the lead film conductors to the pads on the substrate.

The use of a polyimide film as a lead support material is discussed in Section 8.

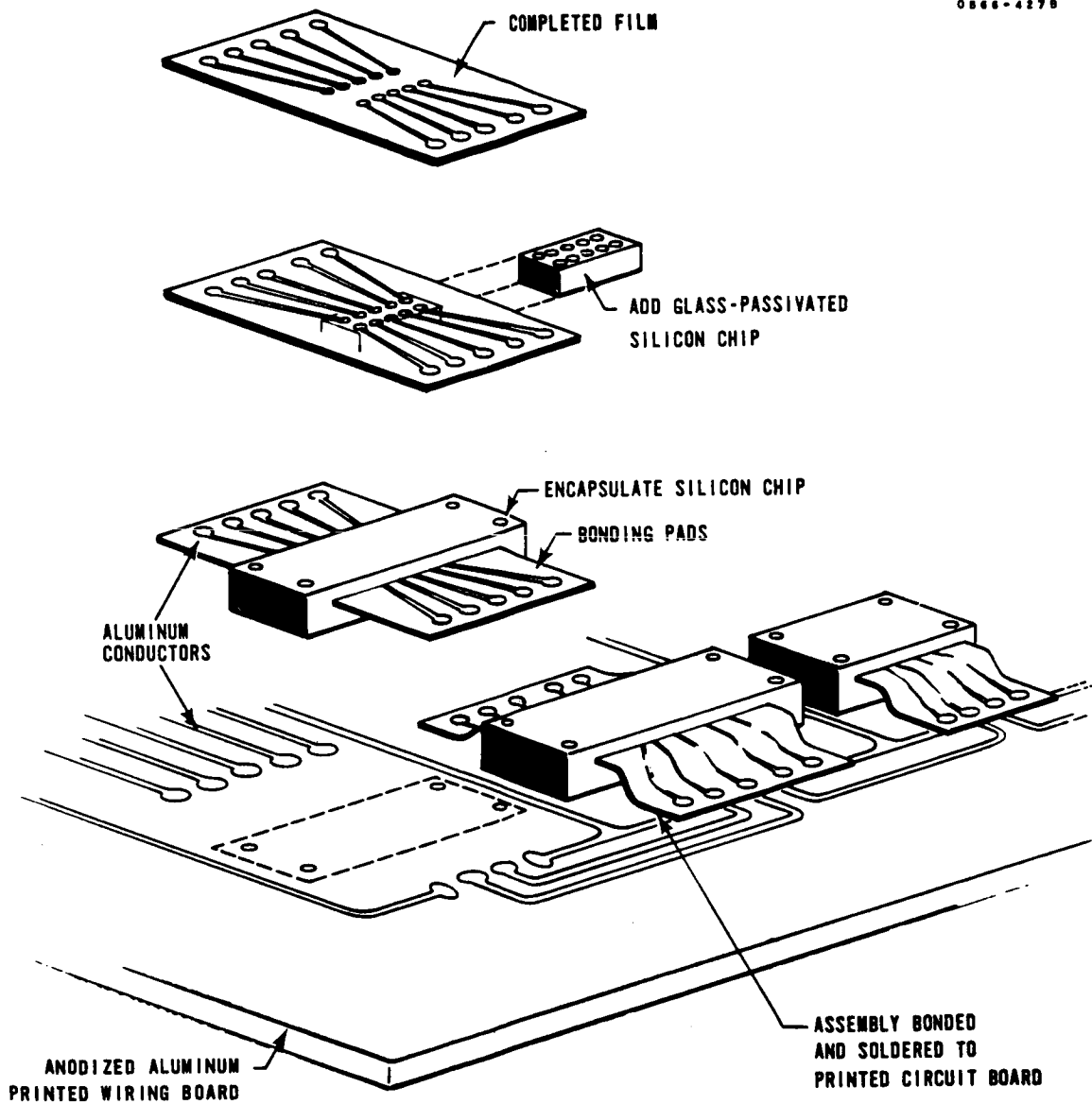* Manufactured by DuPont under the trade name of KAPTON.

FIGURE 18. MONOMETALLIC INTERCONNECTION TECHNIQUE
FOR THE ELIMINATION OF CONDUCTOR INTERFACES

Advantages of Film-Supported Leads - The principal advantages of this technique are:

1. Elimination of flying leads gives support to leads.

2. Prepositioning of leads, eliminating alignment of each individual lead.

3. Testing before assembly is packaged will substantially reduce cost by eliminating rejects after packaging.

4. Several chips can be attached to the lead film with interconnections provided between chips as well as for external connections. Circuit crossovers are the major limitation on the number of chips that can be attached within a single package.

5. The film supported leads along with an anodized aluminum printed wiring board provide a completely monometallic interconnection system.

A plated wire memory plane can be assembled in the same manner as shown in Figure 18. Sufficient space may be allotted on the printed wiring board for the placement of the plated wires and word straps. All the LSIs required for the operation of a single plane can be mounted alongside the memory devices. The interconnection of the LSIs is provided by thin film aluminum conductors which have been deposited on the anodized surface of the aluminum plate. By plating the ends of the memory wires and word straps with a thin film of aluminum, an aluminum-to-aluminum bond can be made between the memory wires and the PWB. Therefore the interconnections between the MOST LSIs and the memory wires is performed by a system completely free of bimetallic interfaces.

8.0 TOTAL REDUCTION OF INTERFACES AND INTERFACE CONNECTIONS

The reduction of interfaces within the memory system envolves all of the following areas:

1. The circuit organization and layout

2. The interconnection of MOS devices within a single chip

3.   The circuit package

4.   The interconnection of MOS circuitry and the plated wire
     stack.

The first three areas are discussed in this section of the report and the
fourth area is discussed in Section 7.

8.1   CIRCUIT ORGANIZATION AND LAYOUT

The area allowing the most progress toward the reduction of interfaces
is the circuit organization and chip layout.   Each MOS chip should con-
tain as much circuitry as practical, being limited only by power dissi-
pation and/or pinouts.   The word driver selection circuitry is used to
describe how interfaces and interconnections can be reduced at the chip
level.   The complete address selection circuitry (including address
register, decoding logic, word drivers, and clock circuits) for 16 words
is shown schematically in Figures 19 and 20.   The selection circuitry
can be expanded to 32 or 64 words by utilizing larger area chips.   The
circuit is constructed entirely of P channel MOSTs, all contained within
the same silicon chip.   The address decoding is mechanized with both
series logic and parallel logic.   The series decoding logic is illustrated
in Figure 19 where the four MOSTs associated with each address are
connected in series.   The parallel decoding logic is illustrated in
Figure 20 where the four MOSTs are connected in parallel.   The series
decoding has the advantage of requiring fewer MOSTs and less chip area
for its implementation.

The four-stage address register has been included as part of the selec-
tion circuitry for two reasons: (1) the total number of conductors into
the memory stack is reduced considerably and as a result the number of
interfaces and interconnections is reduced,   (2) the drive requirements
imposed upon the address register are reduced considerably.   A memory
plane will contain one of these modules for each 16 words and only one
wire for each address bit will be wired into the plane instead of one wire
per word, hence reducing interconnections considerably.   An additional
logic signal will be required to select the proper module and this signal
is coupled into the "Module Select/Read Pulse" circuit.

The decoding logic will be relatively slow due to the high impedance of
the MOSTs used (the higher impedance MOSTs require less chip area),
hence the turn-on time of the output word driver would be much greater

than the required 50 nanoseconds. The 50 nanosecond current fall time is accomplished by the use of a high speed Read pulse which is gated with the decoding logic and the module select signal to turn the word driver off.

The first approximation to the chip size for a 16-word function is shown in Figure 21. Each small block indicates the area required for the respective circuit. It appears entirely feasible that the complete selection circuitry could be contained on a chip 190 mils by 225 mils. A chip of this size can be produced with reasonable yields in the not too distant future. The larger area chips required for 32 and 64 words should become practical within the next two years.

The decoding logic was laid out into more detail as shown in Figures 22 and 23. The individual MOSTs are shown along with the address signal lines. The layout is not drawn to scale and is used for illustration only. It can be seen that the decoding logic can be mechanized with no crossovers, which reduces potential interfaces within the chip.

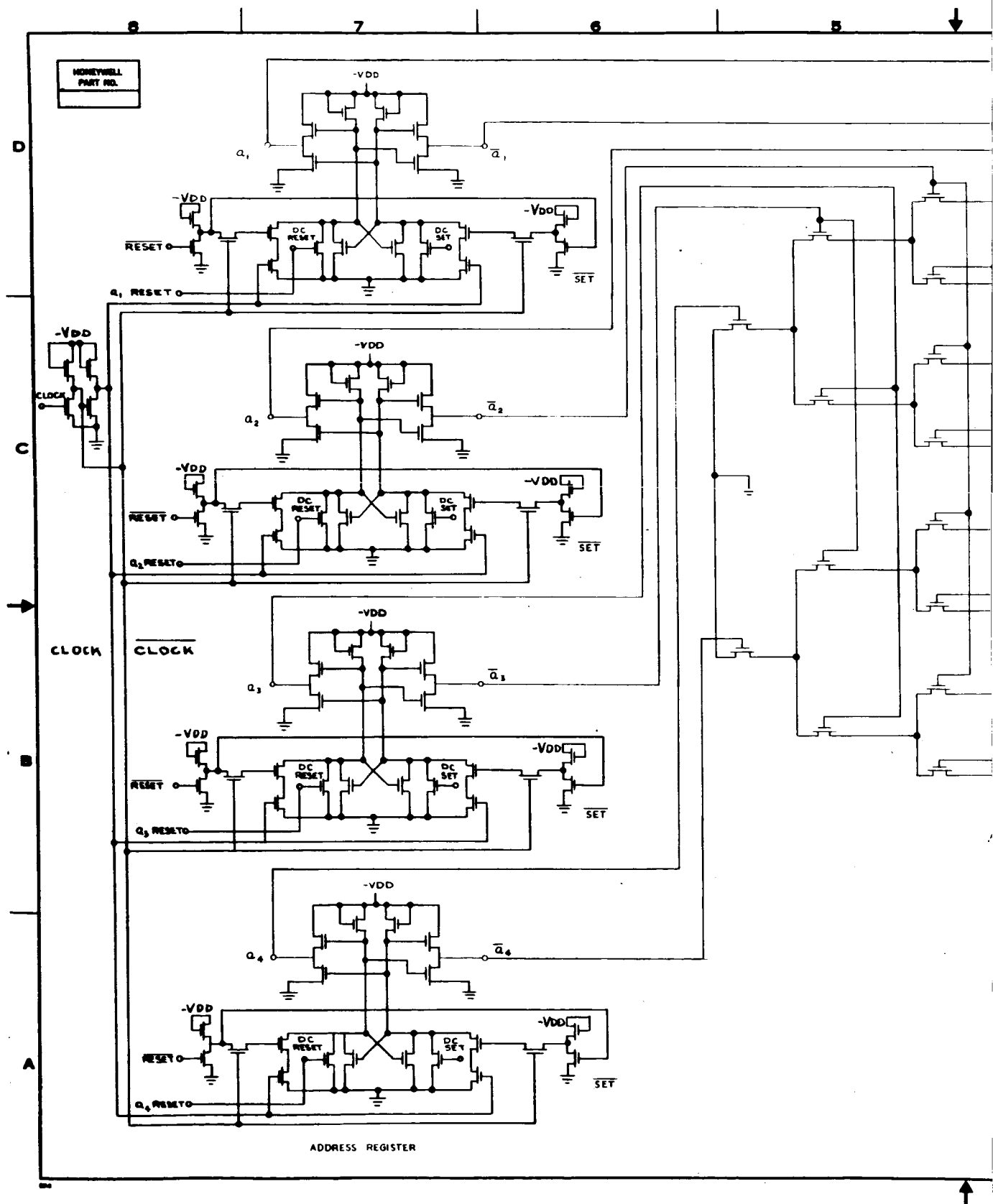## 8.2 REDUCTION OF MOST INTERFACES

The advent of large scale integration (LSI) allows complete functions to be contained within a single chip. Chips containing 1,000 to 2,000 logic type MOS devices become feasible. This reduces the number of interconnections significantly. For example, consider the selection circuitry for 16 words shown in Figure 19. To implement this with normal integrated circuits would require approximately 23 flat-packs of 14 leads each. Fabrication of the complete circuit within a single chip reduces the number of external leads from 182 (for the 23 flat-packs) to 30 for the LSI version, which amounts to a reduction of approximately 85 percent. Increasing the complexity from 16 words to 32 words would allow an even greater reduction. The intraconnections within a device of this complexity is accomplished by a combination of:

Common diffused drain and source regions.

Diffused crossovers (crossunders or tunnels).

Multilayer interconnections on the passivated surface of the chip.
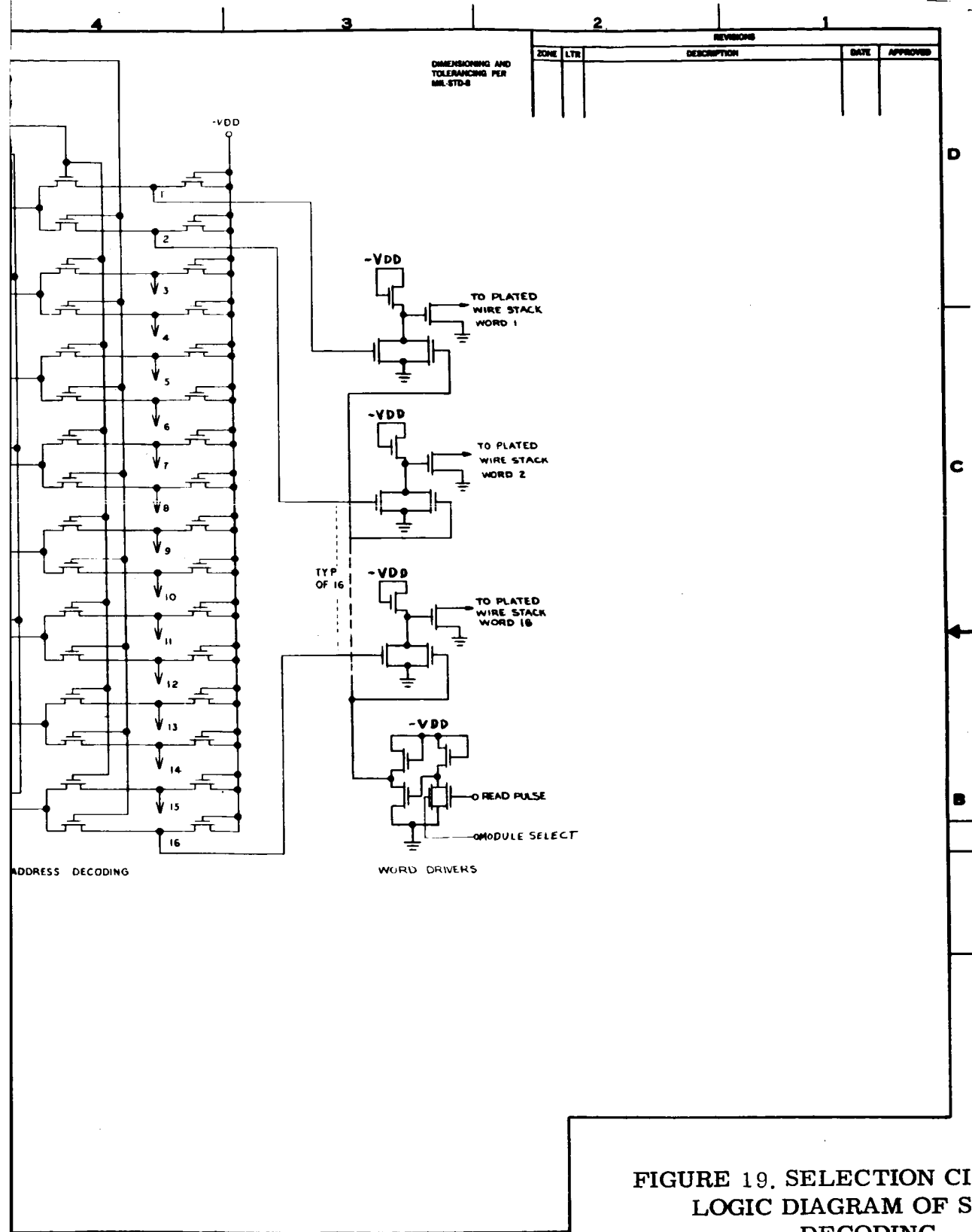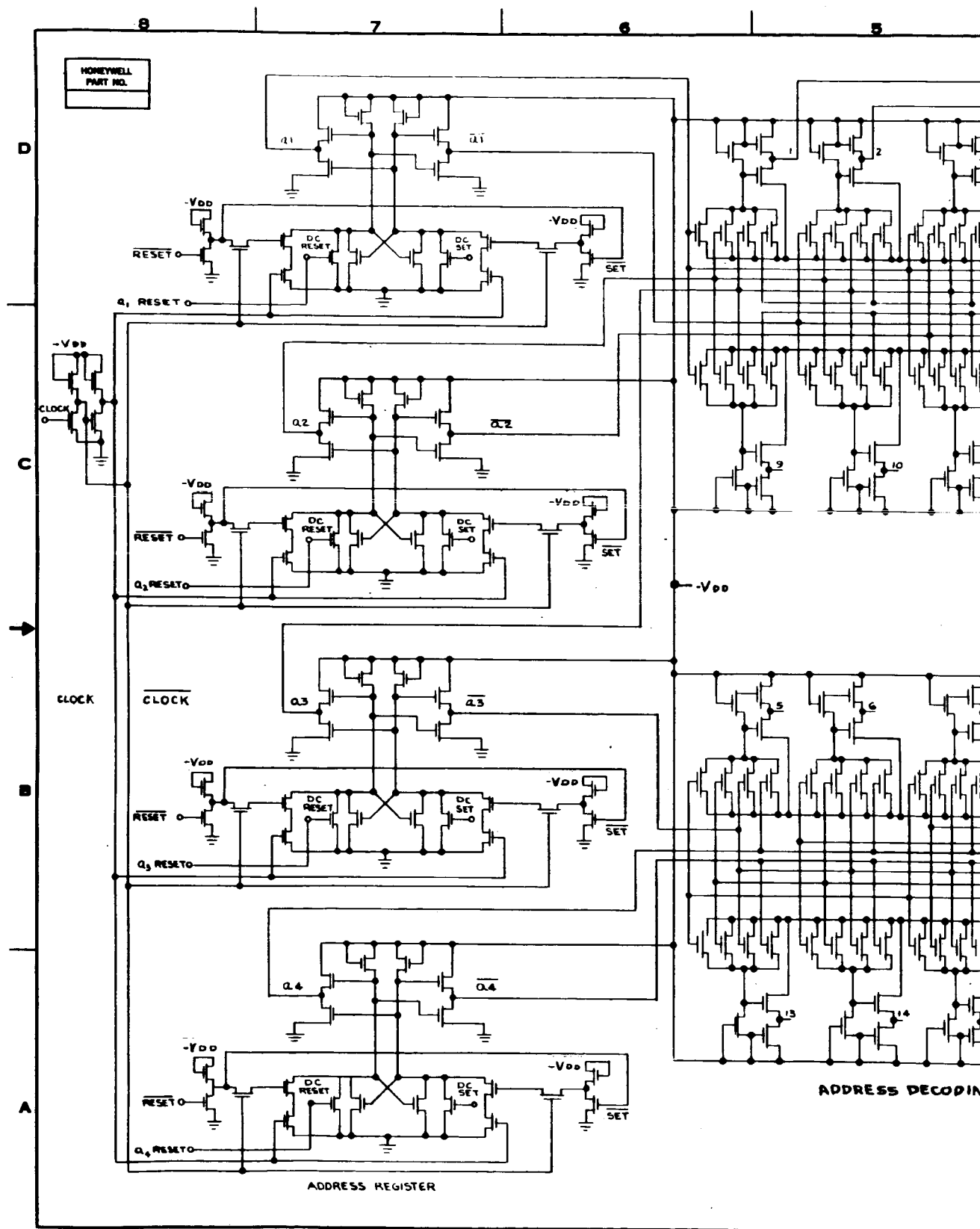
These are discussed in the following paragraphs.

ADDRESS REGISTER

FIGURE 19. SELECTION CIRCUITRY -
LOGIC DIAGRAM OF SERIES
DECODING

ADDRESS DECODING

ADDRESS REGISTER

TO PLATED
WIRE STACK
WORD 1

TO PLATED
WIRE STACK
WORD 2

TYP
of 16

TO PLATED
WIRE STACK
WORD 16

READ PULSE

MODULE SELECT

WORD DRIVERS

FIGURE 20. SELECTION CIRCUITRY -
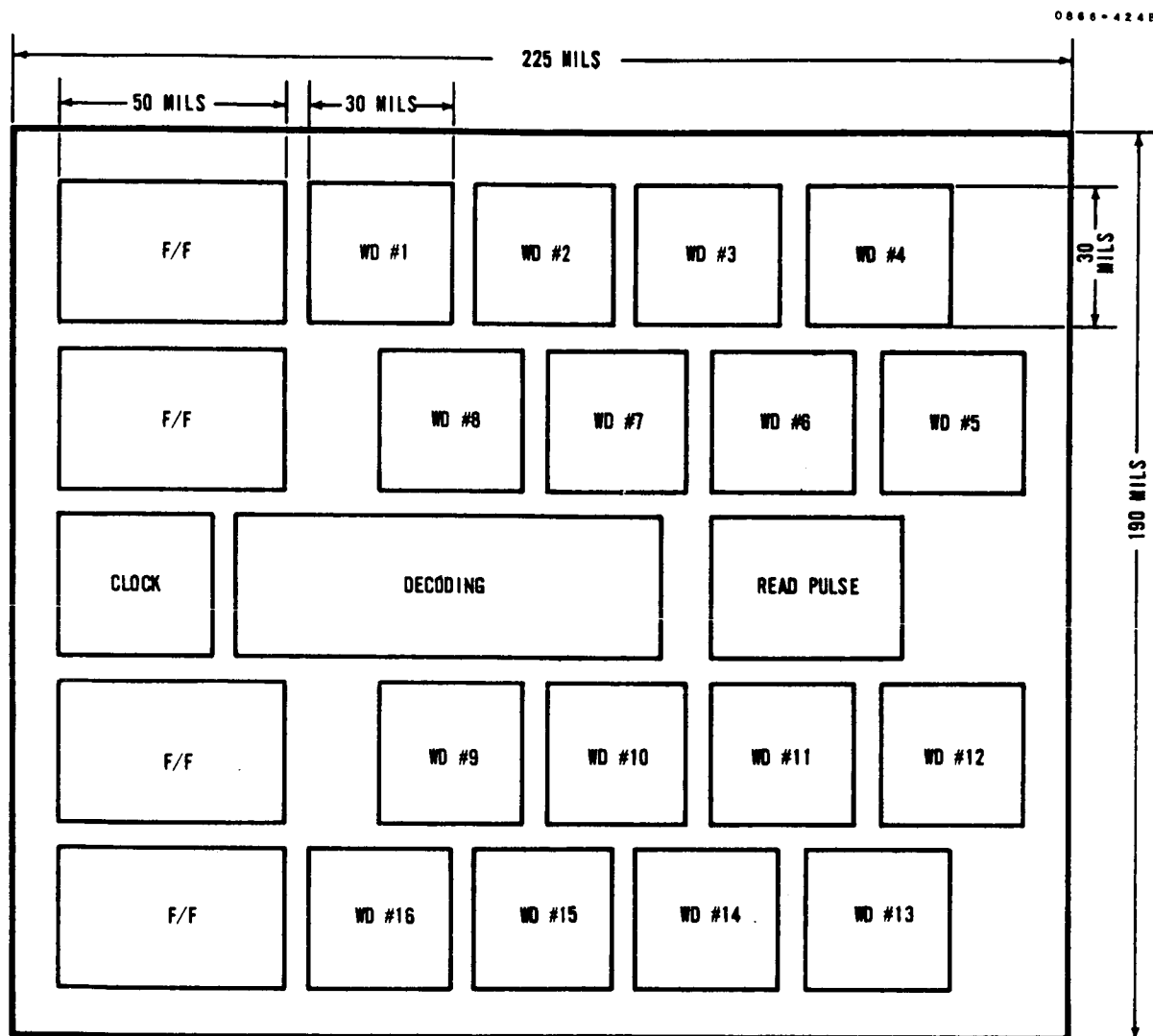LOGIC DIAGRAM OF PARALLEL
DECODING

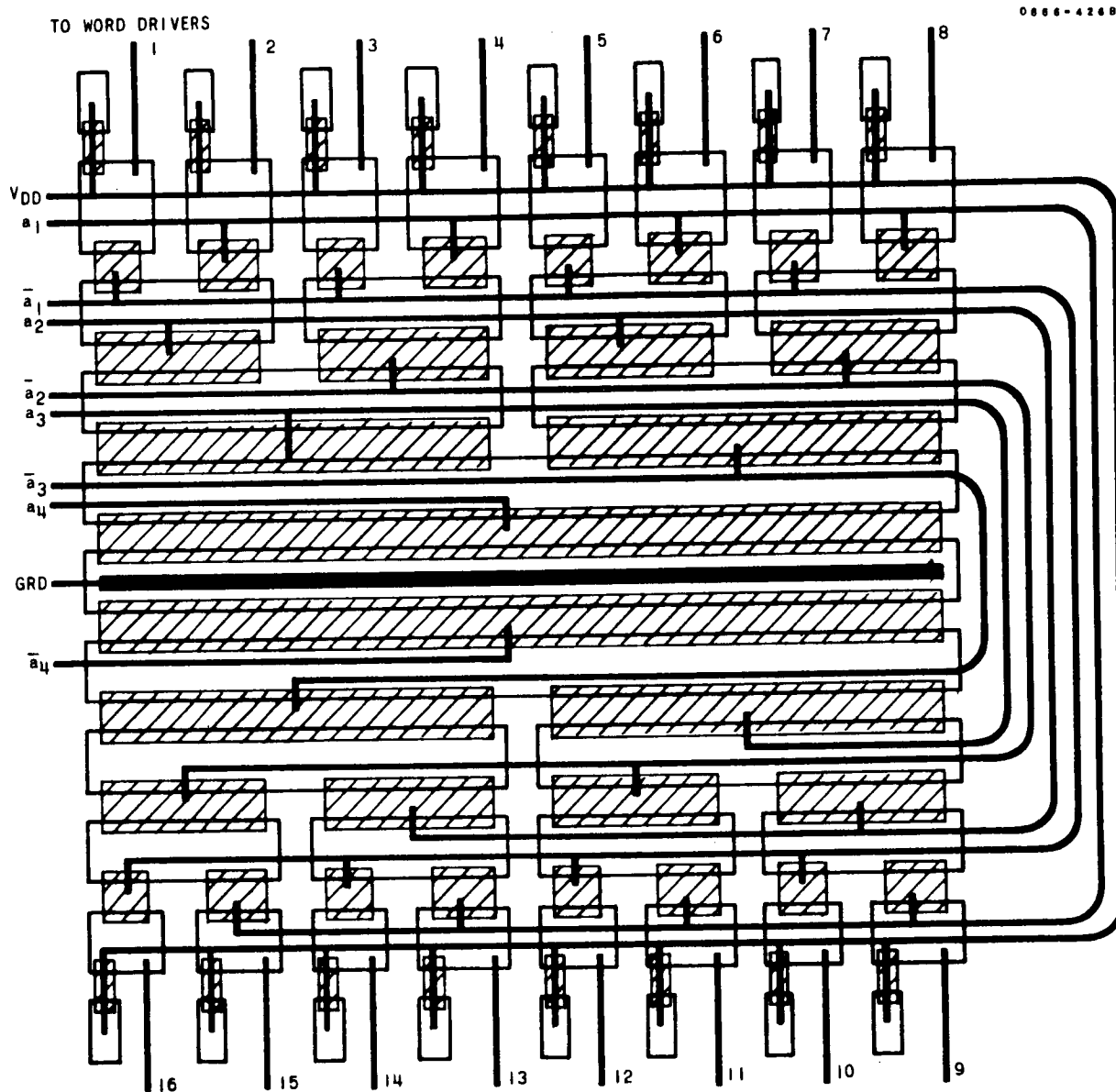FIGURE 21. SELECTION CIRCUIT CHIP - 16 WORDS

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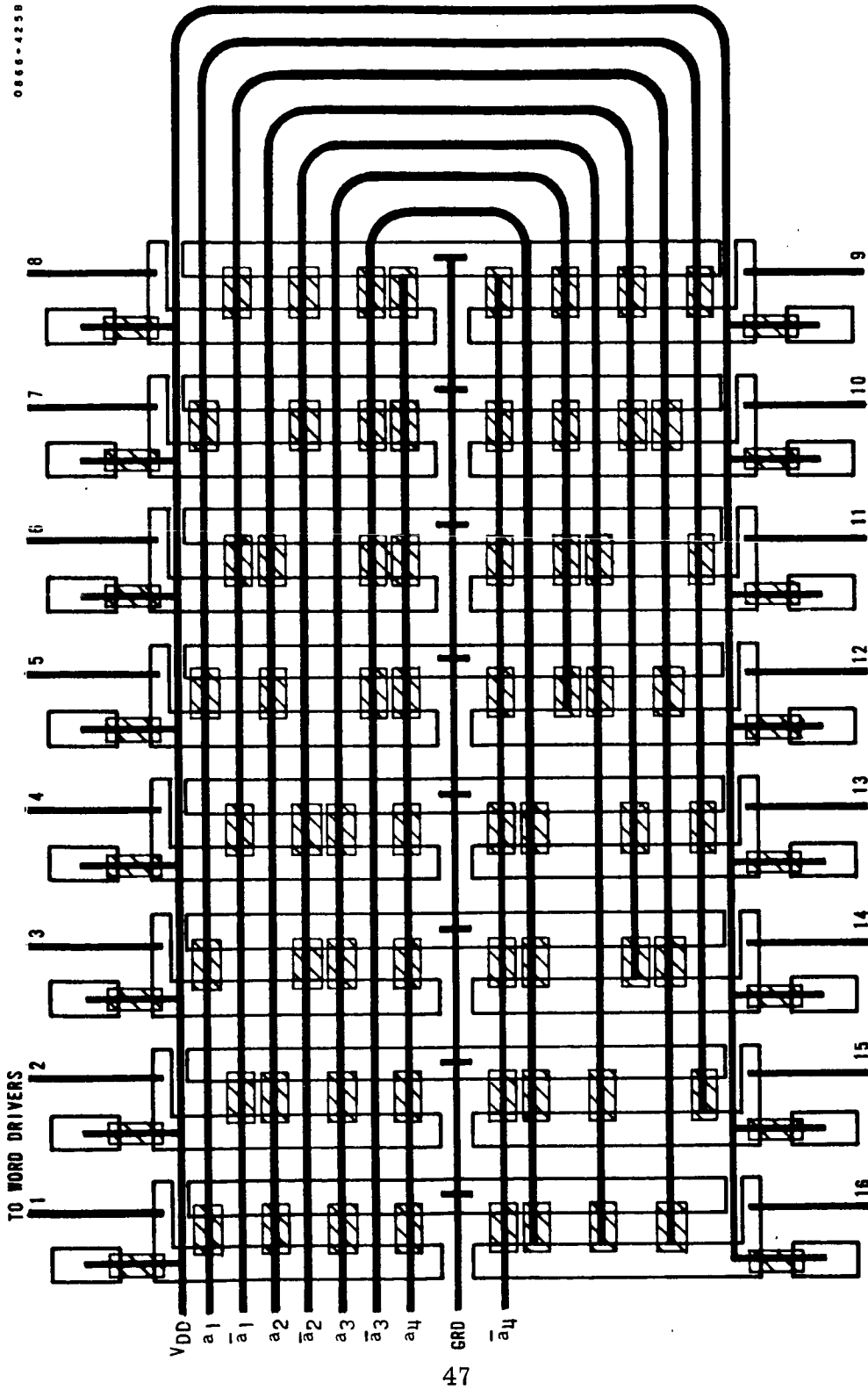FIGURE 22. CHIP LAYOUT OF FOUR-BIT SERIES DECODING

FIGURE 23. CHIP LAYOUT OF FOUR-BIT PARALLEL DECODING

Common Diffused Regions. The MOSTs within the same logic gate may be interconnected by a common diffused region. This is illustrated in Figure 24a where the drain of Q_4 and the source of Q_3 are contained within the same diffused region. This is also true of the drain and source of Q_3 and Q_2 and the drain and source of Q_2 and Q_1. This same figure compares the number of metal-to-silicon interfaces contained in a MOST integrated circuit chip to that of a similar bipolar chip (Figure 24b). There are three metal-to-silicon interfaces in the MOST chip and 18 in the bipolar chip. This is a significant reduction.

Diffused Crossovers. These are sometimes referred to as "crossunders" or "tunnels". In even the simplest integrated circuit it is not always possible to eliminate crossovers. This can be provided by a high concentration diffused region as illustrated in Figure 25. Two conductors, "a" and "b" must cross each other. A P-type isolated region is diffused in the chip during the source and drain diffusion. Contact windows are opened over the left-hand and right-hand sides of the P region in the SiO_2. Circuit continuity for conductor "a" is provided by the diffused P region, hence a "tunnel" is formed. Conductor "b" crosses over the P region as shown and the insulation between "a" and "b" is provided by a thin layer of SiO_2.

The disadvantages of the diffused crossover are increased series resistance and increased stray capacitance. The sheet resistance of a typical source and drain diffusion varies from approximately 100 to 200 ohms per square. This can be reduced to less than 10 ohms per square by an additional P+ diffusion step. The stray capacitance is contributed by the junction capacitance between the P region and the N type substrate. Both of these components tend to reduce circuit speed and increase power dissipation.

Multilayer Interconnections. As the circuit complexity of the chip increases all crossovers cannot be made with the above techniques. More than a single layer of crossovers is required. The interconnections within an LSI are comparable to those of present day multilayer boards. It then becomes necessary to develop a microminiature version of multilayer interconnections which can be deposited on the semiconductor surface and made an integral part of the completed circuit. This required a highly compatible system of metals and insulators.

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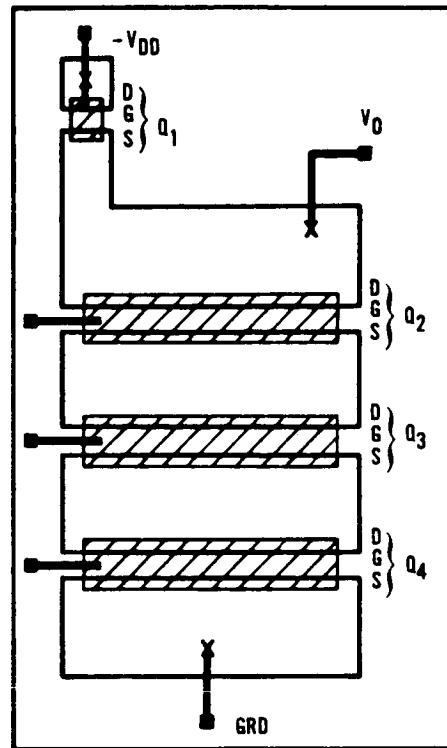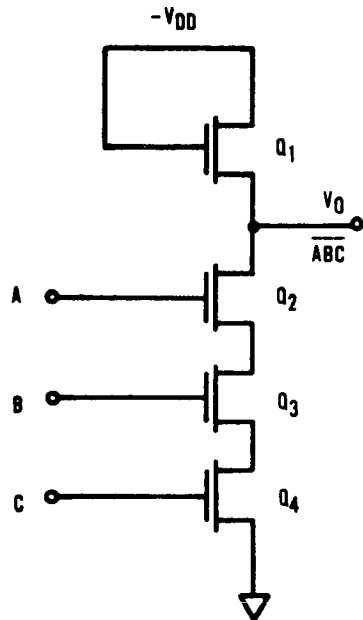
(a) MOST 3-INPUT NAND GATE
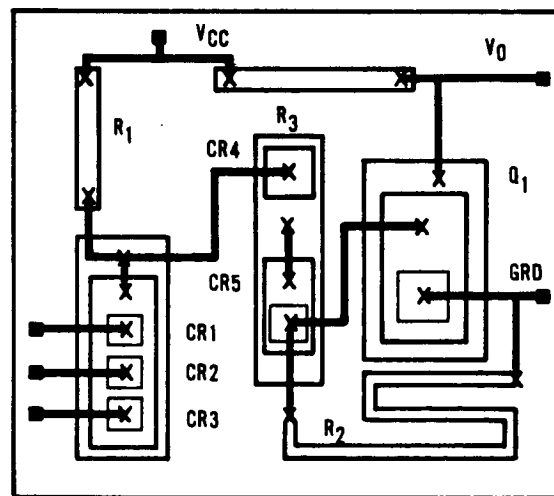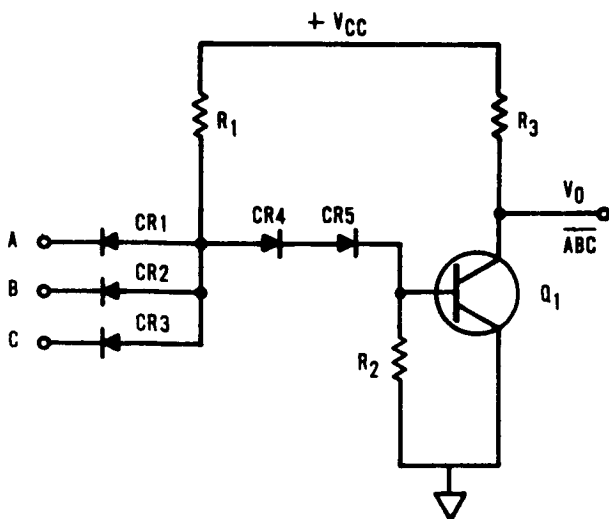
(b) BIPOLAR 3-INPUT NAND GATE

FIGURE 24. A 3-INPUT NAND GATE CONSTRUCTED WITH
BOTH BIPOLAR DEVICES AND MOS DEVICES. (THE METAL-
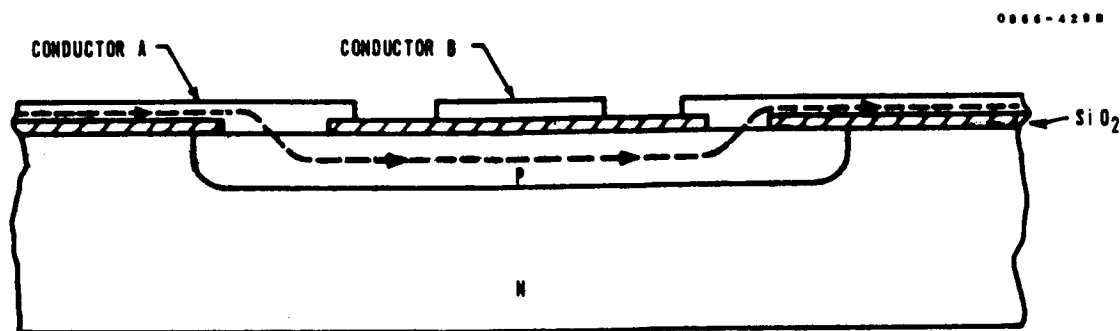TO-SILICON CONTACTS ARE MARKED WITH AN "x".)

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FIGURE 25. CROSS-SECTION OF A SILICON MOST CHIP
SHOWING THE DIFFUSED CROSSOVER TECHNIQUE

The problems associated with utilizing the bimetallic system of gold and aluminum in the interconnection and packaging of transistors and integrated circuits has compelled the industry to develop monometallic systems. A monometallic system becomes even more desirable in the development of multiple layers of conductors on the surface of the silicon chip. The two most practical monometallic systems are all-aluminum and all-gold.

Both of these systems are presently being successfully used by the semiconductor industry in the fabrication of transistors and integrated circuits. The following paragraphs discuss some of the properties of the above systems and some of the methods for providing insulation between conductor layers.

Aluminum has the advantages of adhering well to silicon and silicon dioxide. It is easily evaporated to form a wide range of layer thicknesses; it is a good electrical conductor. It is easily etched with conventional photoresist techniques. It can be bonded by either wedge thermocompression bonding or ultrasonic bonding, and is fairly corrosion resistant. [9] Aluminum also has some shortcomings. A thin layer of oxide rapidly forms on the surface of the aluminum conductor and this requires the bonding process to be very precisely established and controlled to obtain strong bonds between the aluminum film and the aluminum wire. Aluminum requires a completely hermetically sealed package since continued exposure to air, moisture, and other contaminants causes a gradual deterioration of the bonds and thin film conductors. It reacts with the silicon dioxide surface to create inversion layers in the underlying silicon which could be a problem in MOS devices. (The thickness of the SiO_2 layer can normally be made thick enough so that the inversion effects are negligible.)

Gold has the advantages of being completely corrosion resistant, it is easily bonded by thermocompression techniques; it is easily evaporated or sputtered, it is a good electrical conductor; and it is easily etched.[9] Gold, too, has its shortcomings. It does not adhere well to SiO_2 and it reacts with silicon at the eutectic temperature of 370° C. These two problems make it necessary to have an underlying metal layer between the gold and/or silicon and silicon dioxide. Molybdenum and chromium are the two most practical choices. Either one forms a compatible system with gold and silicon. The gold system, using molybdenum as the underlying metal, is fabricated as follows. Molybdenum is deposited on the semiconductor surface by either electron beam evaporation or sputtering. Contact to the silicon is provided in those areas where openings have been opened in the silicon dioxide. Gold is next evaporated over the surface, making good contact with the previous layer of molybdenum. The interconnection pattern is formed by using conventional photoresist techniques and a two step etching process.

The gold interconnect system is presently being pursued for use in LSI circuitry requiring more than a single layer of conductors.

Types of insulating layers investigated and being pursued consist of both organic and inorganic materials. Specifically, they are photoresist, lead monoxide, and silicon monoxide.*

A limited amount of work was performed to determine the feasibility of using photoresist as an insulting medium. A three to four micron film of KTFR was applied to a standard metallized wafer and exposed without a mask. The coated wafer was vacuum baked at 250° C and then 20,000 Å of aluminum was evaporated over the surface. The completed wafer was stored at high temperature to determine if the photoresist would provide insulation between the aluminum layer on top and the metallized devices below. After three days at 300° C, the insulation was still good. The temperature was increased to 325° C, and at the end of 13 days short circuits began to appear as a result of the decomposition of the photoresist. The results indicate that multilayer conductors using photoresists for insulation are probably feasible at lower temperatures and thicker insulating films.

The effort to use lead monoxide (PbO) as the insulating medium was terminated because all of the etchants used to etch the aluminum conductors also attacked the PbO. Aluminum conductors were used in the above investigation because the process for the gold interconnection system has not been completely established.

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* This effort was supported by funds available under a separate contract.

The present multilayer interconnection system being developed consists of SiO as the insulating medium and gold as the conductors with chromium or molybdenum as the underlying metal. The development is in such an early stage that no conclusive results are available, but there are no apparent reasons that the system cannot be perfected.

8.3 AN INTERFACE-FREE PACKAGING CONCEPT

Introduction

A concept for the reduction of interface connections has been conceived and investigated. The concept was implemented in the form of a molecular integrated circuit package (MICPAK) which will interconnect many discrete integrated circuit elements on a single substrate without introducing undesirable interfaces normally found in more conventional packaging. *

In electronic circuit design, two dissimilar packaging interconnection problems are evidenced by digital and analog circuits. In digital circuitry the power requirements are usually low, but the quantity and complexity of interconnection systems can be very large.

Analog circuitry, however, frequently dissipates relatively large amounts of power and presents problems in feedback and shielding, while having straightforward simple interconnection systems.

In the MICPAK concept both of these areas are adequately considered. The substrate is designed with a built-in, low resistivity ground plane over which are routed the electrical circuit conductors formed by conventional photoetch techniques used in the semiconductor industry. This approach provides a comparable technology at the subsystem level to that previously provided at the device components level. The conductor lead inductance, capacitance to ground, resistance, etc., can be optimized for each specific conductor in the circuit.

The material used for the substrate is a high density magnesium oxide which has a layer of metal fused to it to form a ground plane and input/output termination pads. Over this metal film is deposited a dielectric film of silicon monoxide which serves to insulate the subsequent interconnection plane from the ground plane.

Processing of the various planes involved is accomplished by means of photoetching techniques similar to those of the semiconductor industry. A layout is made from which a graphic art drawing is cut to a high degree of precision. This graphic art work is made 50 to 100 times scale and reduced to photo emulsion on a glass plate. Figures 26 through 28 show the substrate, SiO and conductor layout drawings. The conductor plane

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* A large part of this effort was supported by the NAVAL AIR DEVELOP-
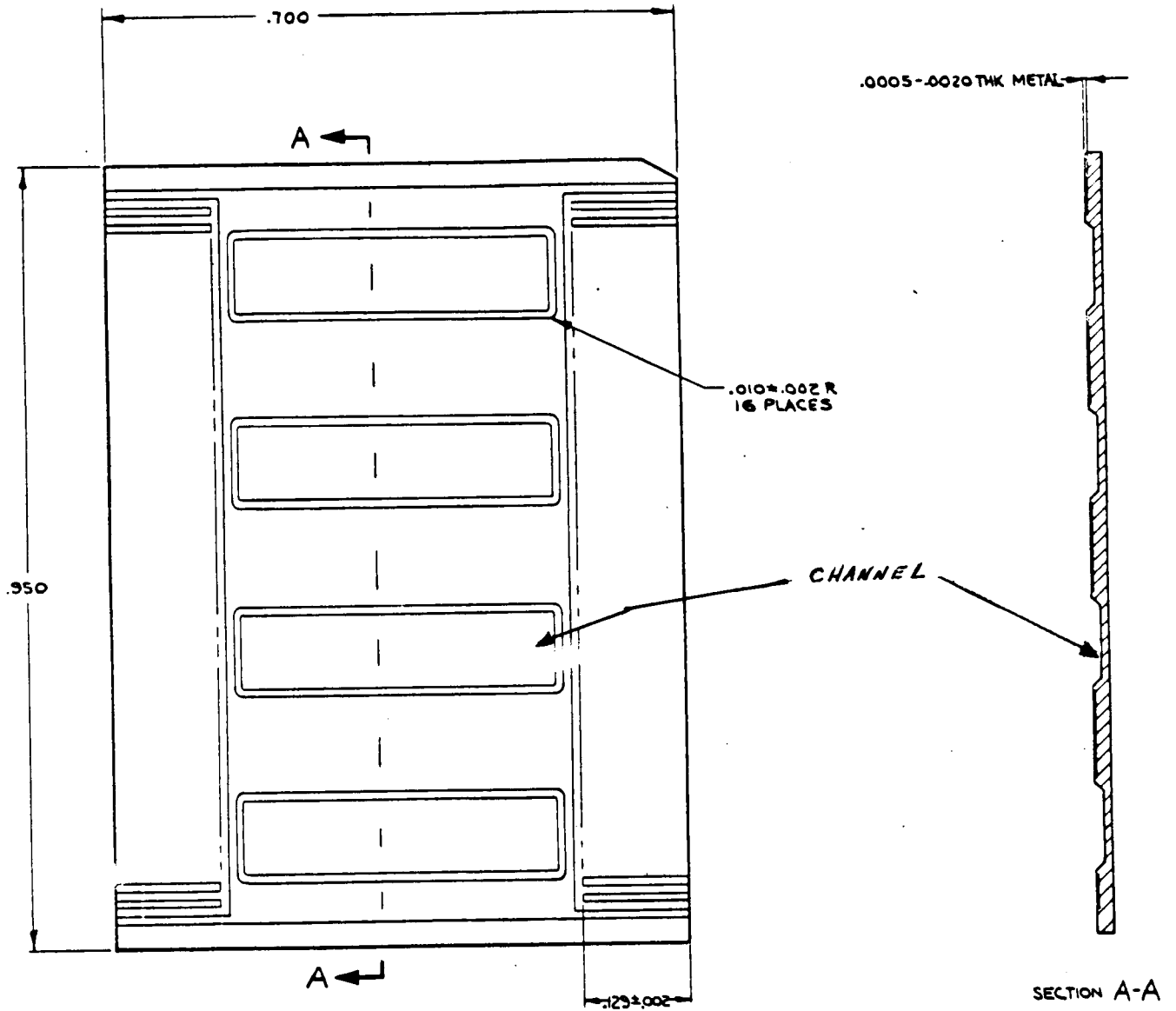 MENT CENTER under contract number N62269-3118.

A6604-69

.0005-.0020 THK METAL

.700

A

.950

.010±.002 R
16 PLACES

CHANNEL

.129±.002

A

SECTION A-A

FIGURE 26.   SUBSTRATE SKETCH
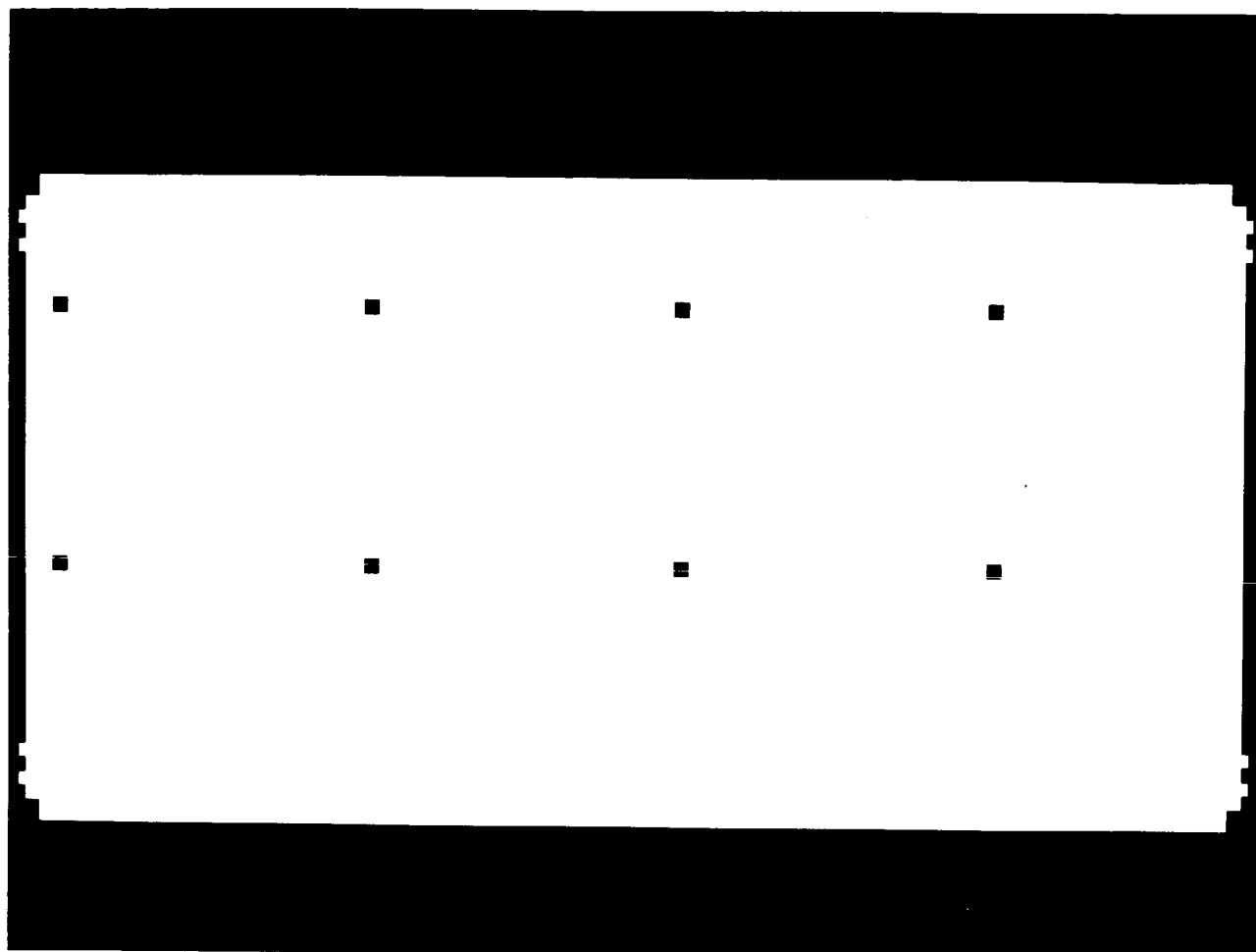
54

A6604-071

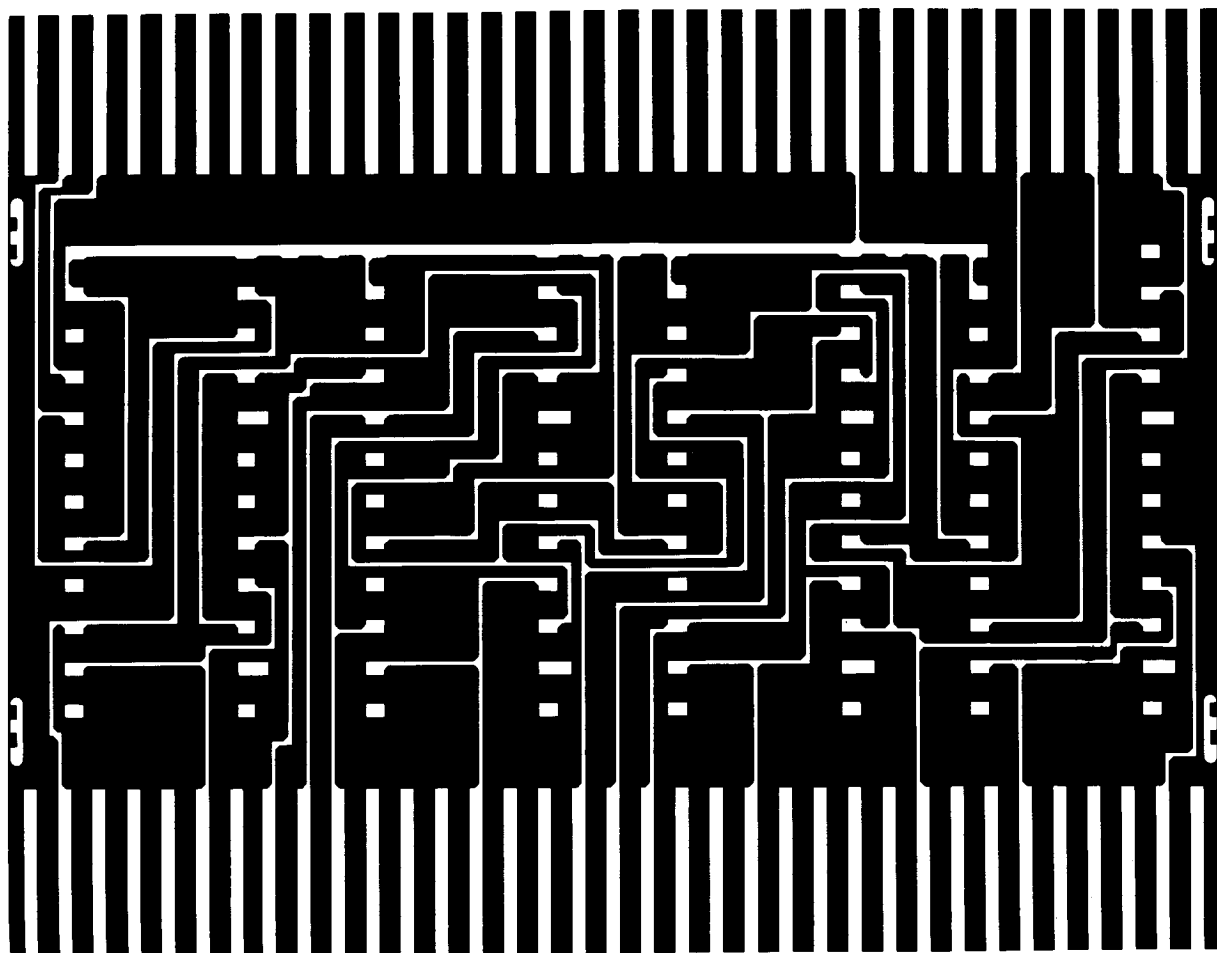FIGURE 27. SiO MASK LAYOUT

A6604-070

FIGURE 28.   CONDUCTOR LAYOUT

is produced by evaporation of a metal film over the SiO which is then etched to the required configuration. Where connection to the ground plane is required the SiO will have previously been etched to produce a window, when the conductor film is evaporated over the SiO the windows will provide electrical connection from the circuit path to the ground plane. Reliability of this connection is assured by alloying the two metals at an elevated temperature.

The integrated circuit dice are mounted in the channels provided by the substrate. The substrate channels are shown in Figure 26 and a cross-sectional view of the mounted dice is illustrated in Figure 29. A feasibility package containing an 8-stage binary counter is shown in Figure 30.

Interconnection Interfaces

A significant failure mode in microcircuitry has been the connection interface between the circuit path and the interconnection lead or conductor. Although basic to electronic equipment fabrication, it is not always recognized that a typical solder connection (Figure 31 shows lead to printed circuit board conductor) has an interface between the conductor and the solder, and another between the solder and the component lead. In Figure 32 (which shows an actual photograph of an eyeleted pc board) there are interfaces between the conductor to solder to eyelet to solder to component lead. Since each interface constitutes a connection, it is the number of interfaces which affect the reliability.

The considerable reliability improvement which has resulted from the introduction of welded interconnection techniques is due in large measures to the reduction in the number of interfaces. Figure 33 shows the weld of a gold plated dumet wire and a nickel ribbon. Although a satisfactory joint was made, an interface can be seen completely across the junction and is typical for this type of interconnection technique. Thermal compression bonding, another microattachment technique, has characteristics similar to those of the welded technique as shown in Figure 34. The number and type of interfaces determines the reliability.

A single NAND circuit was analyzed for various interface connection techniques. For the soldered techniques, 130 interfaces existed; for the welded techniques, 94 interfaces; and for an integrated circuit device with thermal compression bonds, 14 interfaces were required to provide connection to associated circuitry.
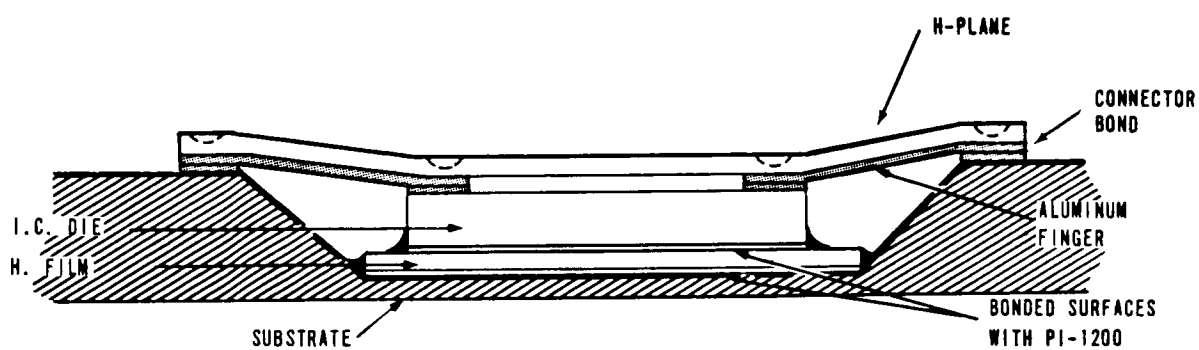
1066-341A

FIGURE 29.   CROSS-SECTIONAL VIEW OF A
SILICON DICE MOUNTED IN A CHANNEL OF THE SUBSTRATE
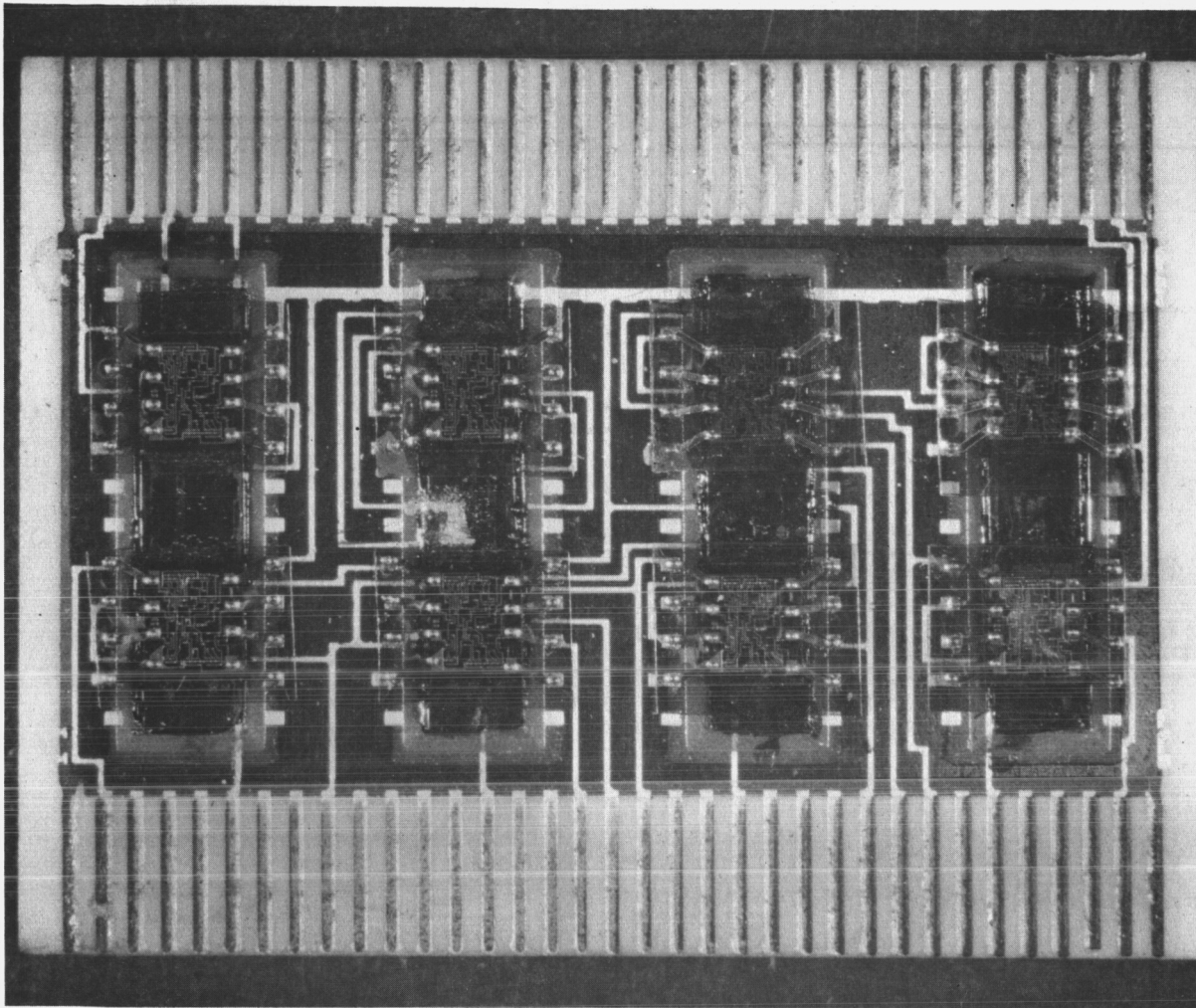
58

A6604-064

FIGURE 30.   COMPLETELY ASSEMBLED PACKAGE
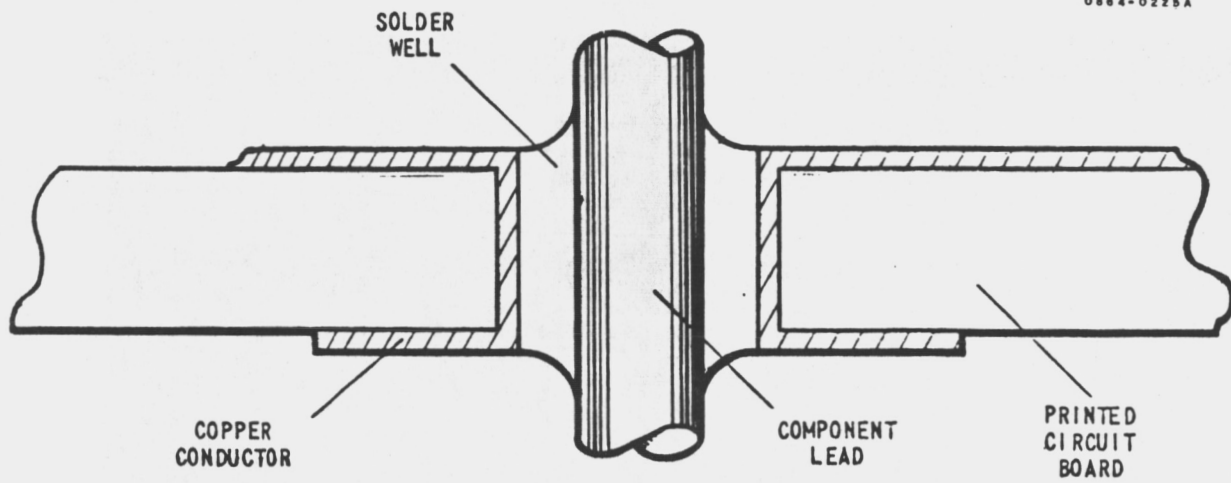PRIOR TO SEALING

0864-0225A

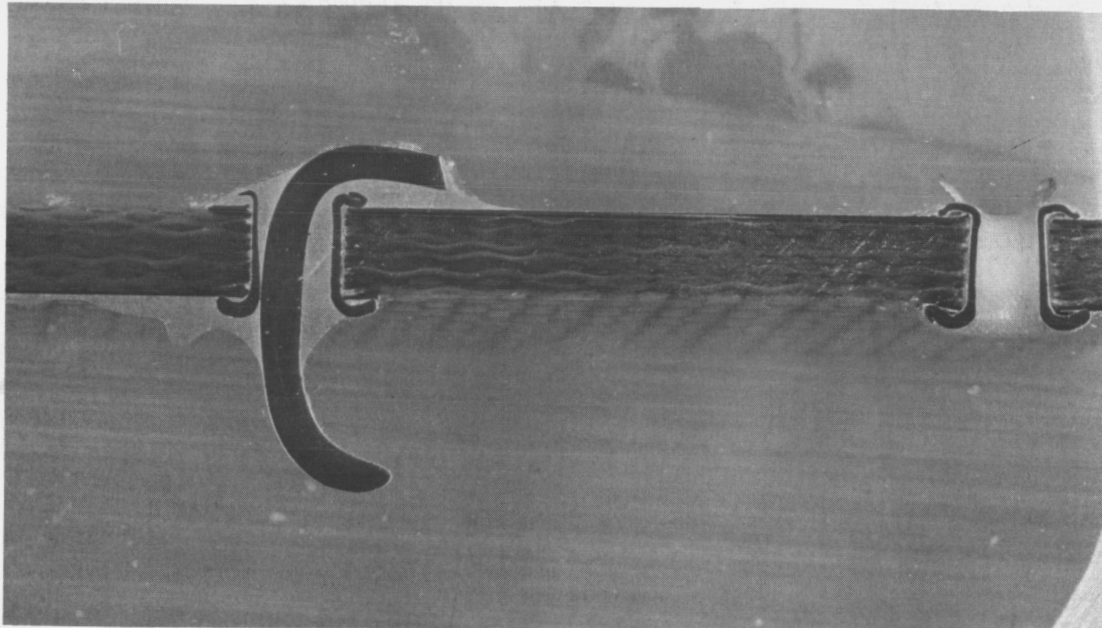FIGURE 31. PRINTED CIRCUIT BOARD SOLDERED CONNECTION

A6402-181-1

FIGURE 32. EYELETED BOND
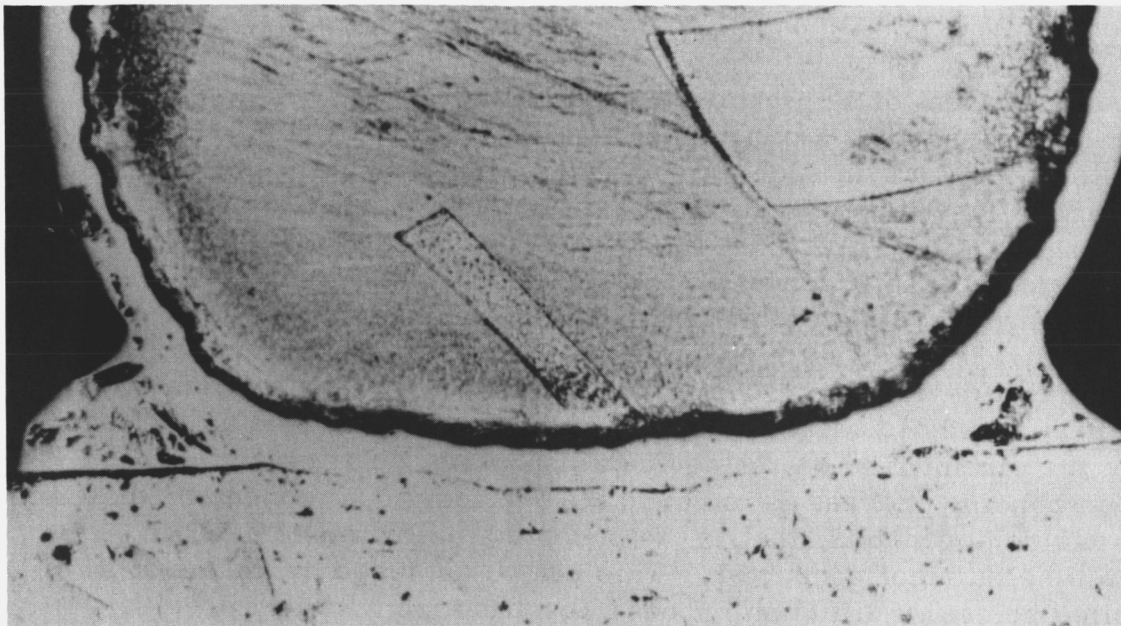
A6 307 02-

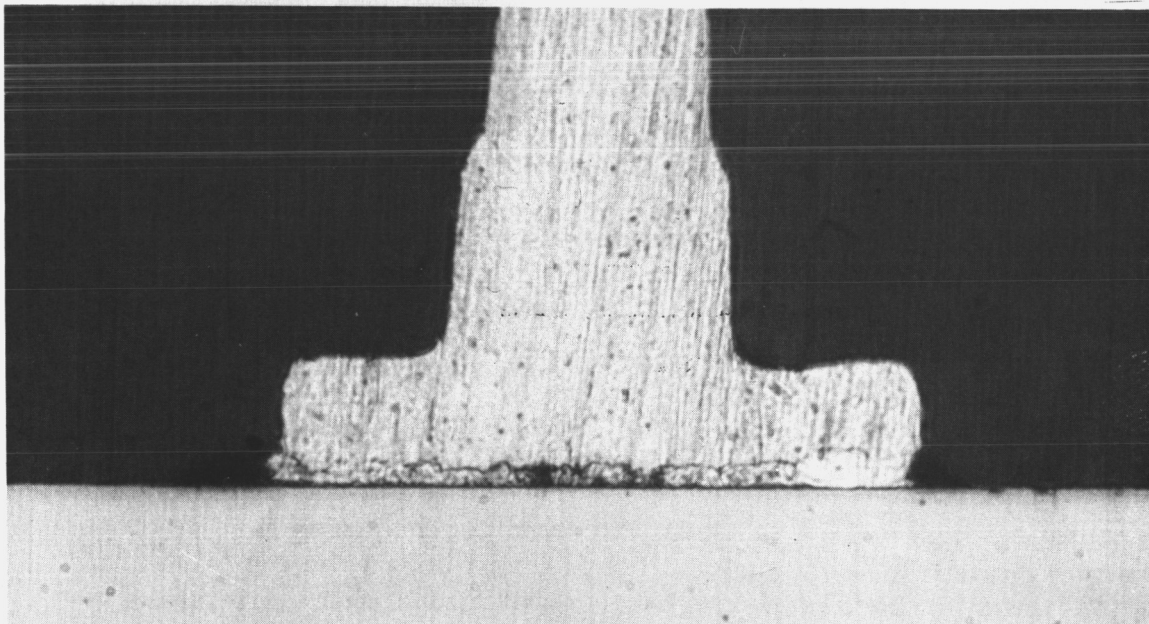FIGURE 33.   WELD BOND

A6403-67

FIGURE 34.   THERMAL COMPRESSION BOND

Intraconnections

In the development of semiconductor technology, a new term, intra-connections, describes a process of connection of two or more points or elements in a circuit in such a manner that the separate connection elements are diffused with NO INTERFACE or change in material composition.

The application of intraconnection techniques to subsystem packages accommodating a variety of separate circuit devices or functions would result in ultra-reliability previously available only within the single integrated circuit device itself. This approach was pursued successfully by producing a highly localized diffusion of the metal film used as the lead wire to the circuit film on the device as substate. The object of the diffusion bonding process is to cause the two individual conductor materials to become homogeneous, that is, to become a single monometallic, monolithic electrical conductor. This can be achieved by means of a controlled selective diffusion process resulting from a very precisely controlled cycle, using relatively thin films (5,000 Å - 100,000 Å).

The conductor material used is a high purity aluminum that is coated onto a conductor support material. This is better understood by referring to Figure 35 which shows a typical diffused joining of the two materials. Figure 35a shows an aluminum conductor on a silicon substrate, and also an aluminum conductor coated onto a conductor support. When the conductor lead is molecularly joined to the conductor on the substrate, the two materials (Figure 35b) diffuse with no detectable interface or composition change. Figure 36 is a microphoto of an actual sectioning of a typical diffused junction produced at Honeywell by this method. No interface is detectable; the material support-lead aluminum coating and substrate conductor have fully diffused; and the lead-support material has also alloyed with the conductor lead. The result is a highly reliable and mechanically strong intraconnection.

Circuit Conductors

The interconnection problem can be largely related to the problem of providing simple reliable crossovers. A crossover requires that circuit paths occur on two planes. In a printed circuit board the two sides of a board with appropriate feedthroughs provide this; in some miniature packages a small wire jumper or flying lead provides the crossover. All of these techniques however require interface connections and additional processing steps. The circuit crossover is accomplished in MICPAK by conductors located in the substrate channels.
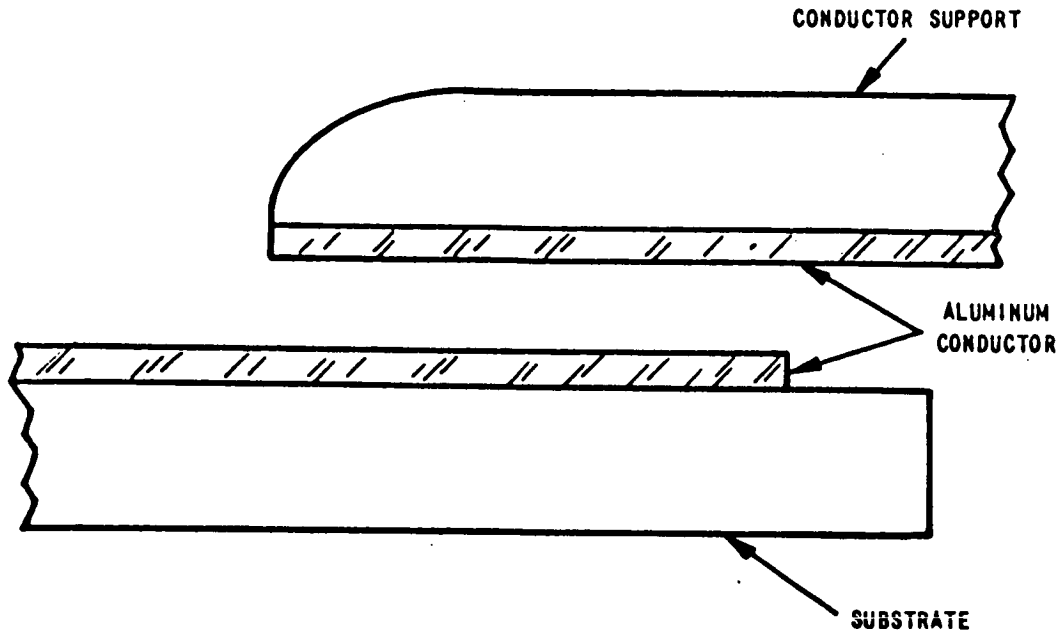
(a) PRIOR TO FUSION
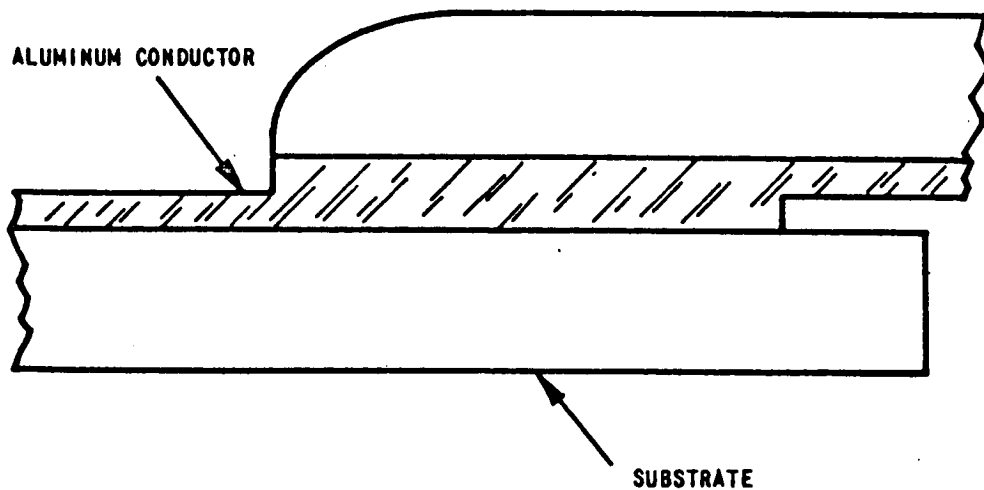
(b) AFTER FUSION
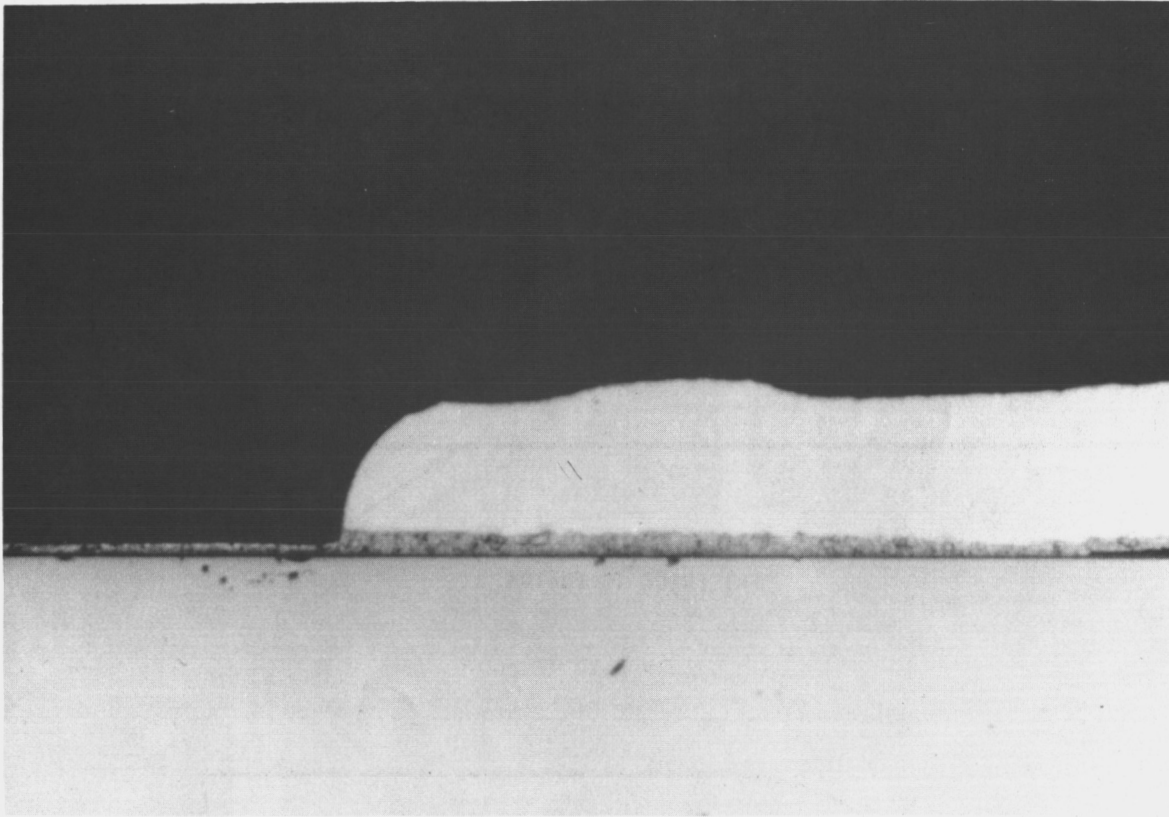
FIGURE 35. SKETCH OF MOLECULAR BOND

A6402-180-1

FIGURE 36.   MICROPHOTO OF MOLECULAR BOND

The channels in the substrate are pressed with the sides formed to a 45-degree angle. This configuration allows the circuitry to be formed continuously both on the surface of the substrate and down into the channels. At each device lead connection the conductor terminates on the substrate at a termination pad. A crossover can therefore be effected by approaching the channel, dropping over the edge and coming back up at a suitable location. This way the circuit path actually occurs on two planes but as may be seen from a top view, from a fabrication viewpoint the circuit is produced in a single step operation with no requirement for an interface since the conductor is continuous.

Interconnection "H" Plane Circuitry

With the die located in a channel a gap exists between the circuitry terminal pads on the substrate and the terminal pads on the die. In practice this gap is approximately 0.010-inch in width and since the conductor films are so thin, requires that they be adequately supported over this area. The three major considerations are those of adequate alignment of the conductor circuitry to the die terminations (16 terminations on a die only 30 x 35 mils are possible), consideration of the thermal expansion characteristics, and diffusion bonding of the various conductors. The conductor support film consists of a polyimide film produced by DuPont called Kapton, or more frequently referred to as "H" film. This material is noted for its inertness and stable high temperature properties. The film is metallized and subjected to photo-processing techniques to produce conductor circuitry which will precisely align with that of the circuit die terminations and also those of the substrate. In general the assembly process consists of diffusion bonding the various die conductors to the "H" film, then mounting the "H" film-die assembly and bonding film conductors to the substrate. This assembly is illustrated in Figure 29. Although there are differences in the coefficients of expansion of "H" film and the other materials, the yield strength of the material permits its use over the temperature range.

Diffusion Bonding

The technique utilized for forming the interface-free bond between the dice and the interconnecting conductors is illustrated in Figure 37. It involves placing the aluminum film side of the metallized H-film in contact with the metallized silicon chip or substrate and simultaneously applying heat and pressure. It is virtually the same as the classic
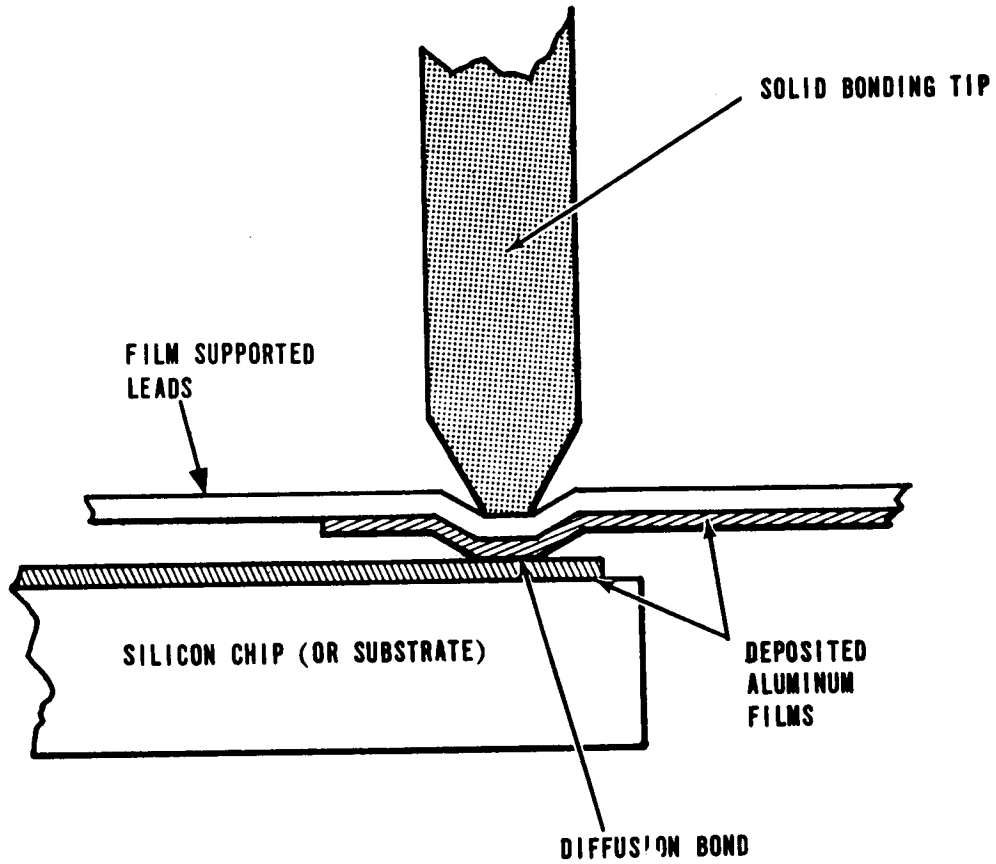
0666-423A

PRIMARY ENERGY SOURCE
SUBSTRATE HEATER

SOLID BONDING TIP

FILM SUPPORTED
LEADS

SILICON CHIP (OR SUBSTRATE)

DEPOSITED
ALUMINUM
FILMS

DIFFUSION BOND

FIGURE 37. H-PLANE DIFFUSION BOND CONCEPT

thermocompression bond. The control parameters were found to be as follows:

Substrate Temperature	360°C
Bonding Tip Geometry	0.004-inch diameter
Bonding Time	10 to 15 seconds

The only source of heat was the substrate heater.

Package Configuration

A complex subsystem package configuration will be defined primarily by: (a) the complexity of the circuit devices and therefore the interconnection system, (b) the number of connections to the outside world (other subsystems or packages outside of the package proper), (c) the area required for the conductor circuitry itself (this includes void areas between circuit conductors). These three items form an optimized relationship to each other.

The complexity of the circuit device is related packaging-wise to the area of the device and the quantity of lead terminations to the device. These lead terminations will be related to the leads required to go to the outside world and will frequently run to 50 or 100 leads for a 1 by 3/4-inch size substrate. A consideration of individual wires or lead ribbons placed serious handicaps on the construction, bonding, and yield of the package. These lead terminations have been made an integral part of the substrate package, providing electrical continuities through the hermetic seal and since the metal is fused to the ceramic substrate there is no danger of the conductor lifting and allowing leakage of the package. A 70-lead package is illustrated in Figure 38.

Future Circuit Packaging

The interface-free techniques discussed above are applicable to the packaging of Large Scale Integrated (LSI) circuits. LSIs are monolithic integrated circuits containing typically 100 to 200 logic gating functions. These monolithic chips can vary in size from 50 mils in a side to 500 mils on a side. By utilizing diffusion bonding of aluminum to aluminum conductors deposited on "H" film complete LSIs can be packaged as shown in Figure 18. The illustration uses a typical integrated
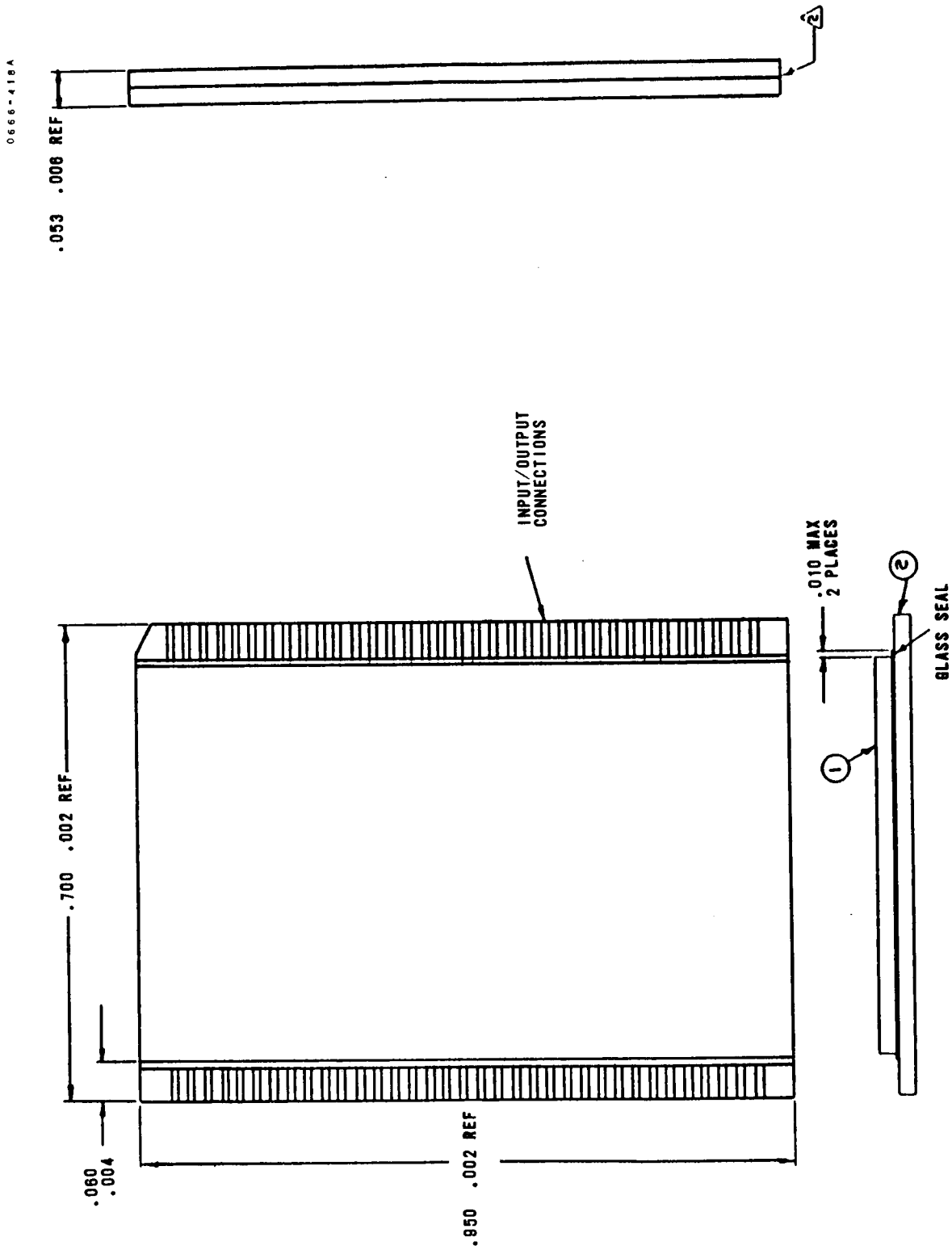
FIGURE 38. A 70-LEAD INTEGRATED CIRCUIT PACKAGE

INPUT/OUTPUT CONNECTIONS

GLASS SEAL

.010 MAX
2 PLACES

.700 .002 REF

.060 .004

.850 .002 REF

.053 .006 REF

0666-418A

circuit but the same concept applies to LSIs with 50 to 100 pinouts. The assembly process, briefly stated, is:

1. Evaporate the conductor onto the film.

2. Photoetch the desired interconnect pattern into the conductor metal in a manner analogous to making flexible printed circuits.

3. Bond the aluminum conductors on the film to the contact pads on the chip using thermocompression or ultrasonic bonding.

4. Electrically test the chip/lead film assembly.

5. Package completed assembly.

6. Assemble the packaged circuits onto the anodized printed wiring board (PWB) and attach the lead film conductors to the pads on the substrate.

The film supported leads along with the anodized aluminum printed wiring board provides a completely interface-free interconnection system.

The use of LSIs and film supported leads increases the reliability of the system considerably.

9.0 MANUFACTURING COMPATIBILITY OF THE MAGNETIC WIRE AND THE MOS DEVICES

The results of this contract have shown plated wire memories with MOS electronics to be entirely feasible. Nowhere do the results indicate the existence of any manufacturing incompatibilities between the plated wire and the MOS devices. Instead, their manufacturing methods indicate a very high degree of compatibility since each is produced by completely separate and isolated processes. Both the plated wire and the MOS devices are fabricated, tested, and assembled in their own subassembly prior to being integrated into a working memory system. Each of the manufacturing processes are discussed briefly in the following paragraphs.

9.1 MOS MANUFACTURING PROCESS

The processes involved in the fabrication of N and P channel MOSTs, and MOSTs with bipolar transistors are outlined briefly below. The discussion begins with a simple single-type device and progresses to a complex chip containing both N and P type MOSTs and isolated NPN bipolar transistors. All MOSTs are considered to be enhancement mode devices unless otherwise noted.

The basic steps in the fabrication of MOS monolithic subsystems and conventional double-diffused integrated circuits are the same except that (1) the sequence of steps is repeated less often in the MOS technology; (2) the growth of an epitaxial crystal layer is omitted in the MOS; and (3) only one diffusion is required rather than four as in the conventional double-diffused process.

P Channel MOST. The cross-section of a P channel MOST is shown in Figure 39. The N type starting material is normally in the range of
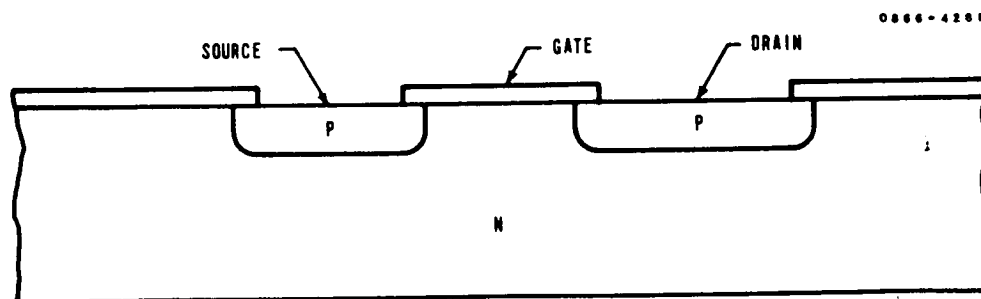

FIGURE 39. SKETCH OF P CHANNEL ENHANCEMENT MODE MOST CHIP

3 to 20 ohm-cm, and the drain and source is normally diffused to a surface concentration of 10^{17} to 10^{20} atoms/cm^3. The gate oxide is 1000 to 2000 Å thick and the gate threshold voltage varies from -3 to -6 volts. The threshold voltage is difficult to predict accurately because it is a function of the charges present at the surface and within the body of the silicon material. These charges are a result of fixed impurity ions within the body, the abrupt termination of the silicon crystalline structure at the surface, and ions contained within the silicon dioxide above the channel region. The process sequence for a P channel MOS device is described in the following paragraphs.

The process starts with an N-type silicon slice which is first oxidized to form a layer of silicon dioxide and then coated in a dark room with a photo-sensitive material. This material is exposed to light through a high-resolution mask. The portions not exposed are soluble and easily removed by a solvent rinse. An etch is used to dissolve the silicon dioxide from the areas not protected by the film of photosensitive material. The wafers are then placed in a special high-temperature furnace containing an atmosphere of gaseous boron (P-type impurity). The boron impurity diffuses into the surface of the silicon wafer only where the oxide has been removed, forming the P-type source and drain. Even at elevated temperatures the oxide protects the surrounding areas from the dopants. A new layer of oxide is formed over the exposed silicon areas of the source and drain during the diffusion.

The desired oxide thickness in the gate region is obtained by removing part of the oxide by the same masking and etching techniques. Portions of the source and drain are then exposed by masking and etching, and a layer of aluminum is deposited over the entire surface, contacting the exposed silicon at the source and drain. The metal surface is then selectively removed. Only the interconnection pattern, source and drain contacts, and gate metallization are left.

Briefly, the process steps and the number of masks required in the fabrication of the P channel MOST are:

1. Source and drain oxide removal (Mask No. 1).

2. Source and drain diffusion.

3. Gate oxide formation (Mask No. 2).

4. Source and drain contact oxide removal (Mask No. 3).

5. Metallization (Mask No. 4).

N Channel Enhancement Mode MOST. The fabrication of enhancement mode N channel MOSTs can be accomplished by either of two approaches: (1) the starting material is relatively low resistivity (0.2 to 0.5 ohm-cm) and the source and drain are diffused as shown in Figure 40; (2) the
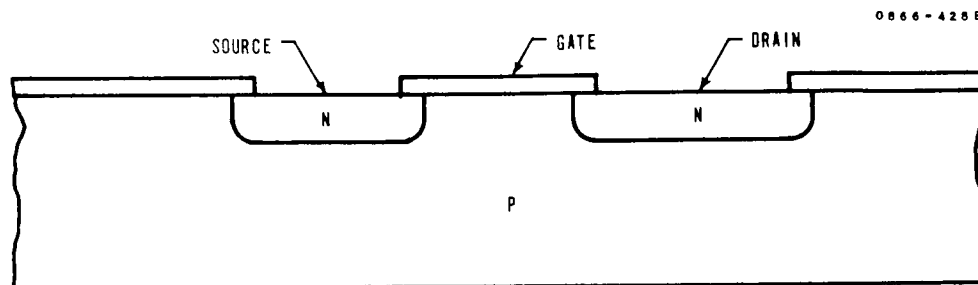

FIGURE 40. SKETCH OF N CHANNEL ENHANCEMENT
MODE MOST CHIP USING P TYPE STARTING MATERIAL

starting material is high resistivity (10 ohm-cm) N type with diffused P type isolation regions for location of the N channel MOSTs as shown in Figure 41. Both of these approaches provide a surface concentration in
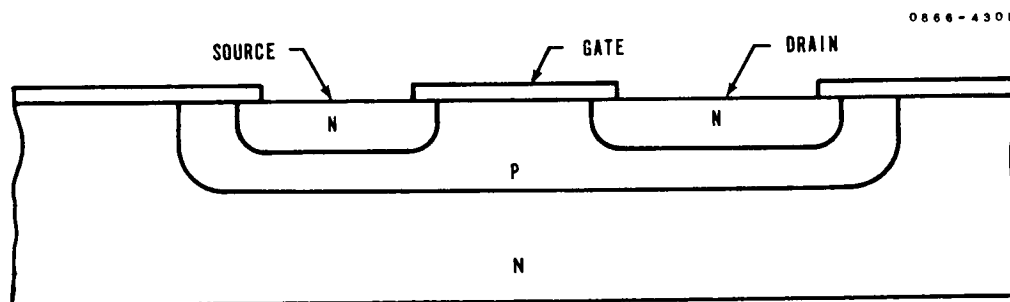

FIGURE 41. SKETCH OF N CHANNEL ENHANCEMENT MODE
MOST CHIP USING N TYPE STARTING MATERIAL

the P regions greater than $5 \times 10^{16}/cm^3$, which is necessary to prevent the formation of undesirable inversion layers. The process steps for the first approach (P type starting material) are:

1. Source and drain oxide removal (Mask No. 1).

72

2. N type source and drain diffusion.

3. Gate oxide formation (Mask No. 2).

4. Source and drain contact oxide removal (Mask No. 3).

5. Metallization (Mask No. 4).

The process steps for the second approach (N type starting material) are:

1. Isolation region oxide removal (Mask No. 1).

2. P type isolation diffusion.

3. Source and drain oxide removal (Mask No. 2).

4. N type source and drain diffusion.

5. Gate oxide formation (Mask No. 3).

6. Source and drain contact oxide removal (Mask No. 4).

7. Metallization (Mask No. 5).

N Channel Depletion Mode MOST. The fabrication of depletion mode N channel MOSTs requires a P type surface concentration of $<< 5 \times 10^{16}/cm^3$. This allows the channel region to automatically invert to an N type surface, hence a depletion mode device is formed. The entire P type surface will also invert, generating leakage paths between source and drain of the same device and between devices on the same chip. This can be avoided by the fabrication technique illustrated in Figure 42. Here a P+ guard band with a surface concentration of greater than $5 \times 10^{16}/cm^3$ is diffused around each source and drain to terminate any inversion layers that may be formed. A P type concentration greater than $5 \times 10^{16}/cm^3$ is sufficient to prevent inversion of the surface to N type. The process for fabricating depletion mode N channel MOSTs is:

1. Guard band oxide removal (Mask No. 1).

2. P type guard band diffusion.

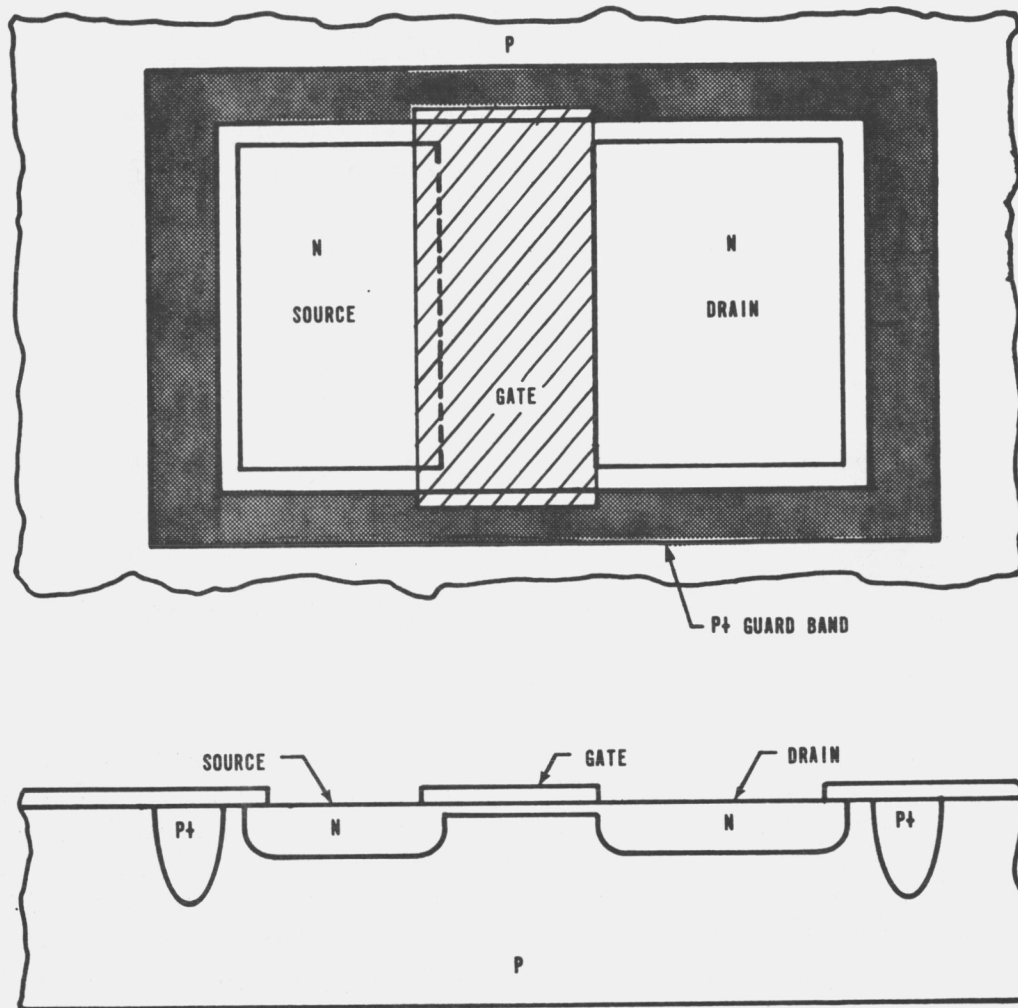3. Source and drain oxide removal (Mask No. 2).

73

0866-430B

FIGURE 42.   A DEPLETION MODE N CHANNEL MOST
UTILIZING A P+ GUARD BAND FOR CONTROLLING
SURFACE INVERSION BETWEEN SOURCE AND DRAIN

4. N type source and drain diffusion.

5. Gate oxide formation (Mask No. 3).

6. Source and drain contact oxide removal (Mask No. 4).

7. Metallization (Mask No. 5).

P Channel MOST With Common Collector NPN. The cross-section of a chip containing P channel MOSTs and common collector NPN bipolar transistors is shown in Figure 43. Using N type starting material, the
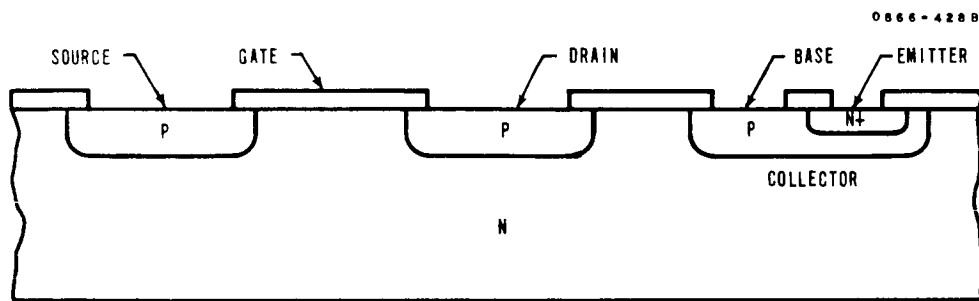

FIGURE 43. SKETCH OF P CHANNEL MOST AND BIPOLAR NPN TRANSISTOR (COMMON COLLECTOR) IN THE SAME CHIP

process steps for the fabrication of this device are:

1. Source, drain, and NPN base oxide removal (Mask No. 1).

2. P type source, drain, and NPN base diffusion.

3. NPN emitter oxide removal (Mask No. 2).

4. N+ emitter diffusion.

5. Gate oxide formation (Mask No. 3).

6. Contact oxide removal (Mask No. 4).

7. Metallization (Mask No. 5).

P Channel MOST With NPN. A more versatile combination of MOSTs and bipolar transistors is illustrated by the chip cross-section shown in Figure 44. Here each bipolar transistor contains its own collector region.
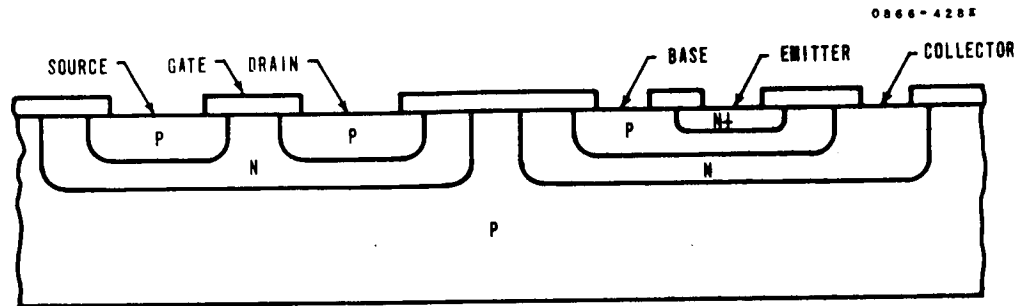

FIGURE 44. SKETCH OF ISOLATED P CHANNEL MOST AND
NPN BIPOLAR TRANSISTOR IN THE SAME CHIP

Using P type starting material and all-diffusion techniques, the process steps for the fabrication of this device are:

1. NPN collector and MOST isolation region oxide removal (Mask No. 1).

2. N type collector and MOST isolation diffusion.

3. Source, drain, and NPN base oxide removal (Mask No. 2).

4. P type source, drain, and NPN base diffusion.

5. NPN emitter oxide removal (Mask No. 3).

6. N+ emitter diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

Complementary MOSTs. The integration of both N and P type MOSTs within the same chip is illustrated by the cross-section shown in Figure 45.
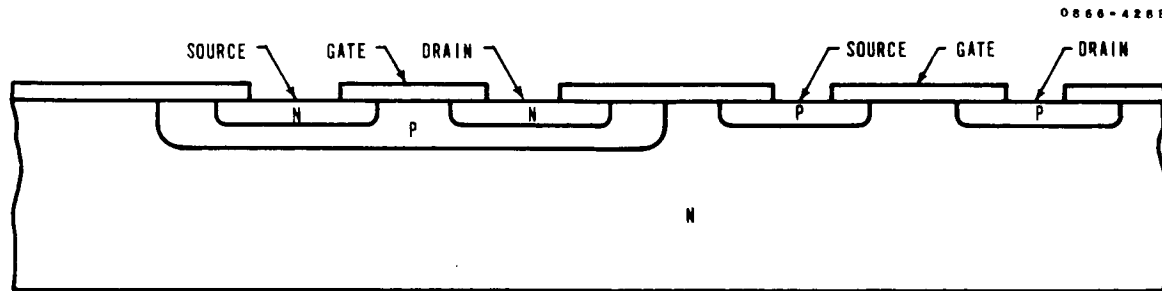

FIGURE 45. SKETCH OF COMPLEMENTARY P CHANNEL AND
N CHANNEL MOSTs IN THE SAME CHIP

The desirability of complementary MOSTs is discussed in another section of this report. The simplest fabrication process uses N type starting material and is:

1. N channel isolation region oxide removal (Mask No. 1).

2. P type isolation diffusion.

3. P channel source and drain oxide removal (Mask No. 2).

4. P type source and drain diffusion.

5. N channel source and drain oxide removal (Mask No. 3).

6. N type source and drain diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

The parameters of each type of MOST can be improved at the expense of additional process steps in the formation of the channels, gate oxide, and the metallization. This would require at least two additional masking operations.

Complementary MOSTs and Bipolar NPNs. The fabrication of comple-
mentary MOSTs and bipolar NPN transistors within the same silicon chip
can be accomplished by either of two approaches:

All diffused.

Epitaxial diffused.

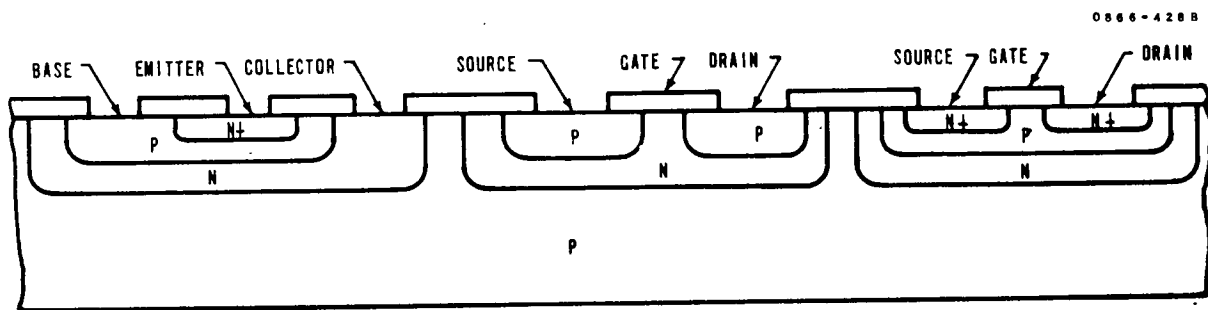The all-diffused approach is shown in Figure 46. This process can provide

0866-4268

FIGURE 46. SKETCH OF COMPLEMENTARY MOSTs AND
NPN BIPOLAR TRANSISTOR IN THE SAME CHIP

functions with the capability of high operating speeds and low power dissi-
pation. The process uses a P type substrate and the steps are:

1. Oxide removal for NPN collector and MOST isolation (Mask No. 1).

2. N type diffusion.

3. Oxide removal for NPN base, N channel MOST isolation, and
   P channel source and drain (Mask No. 2).

4. P type diffusion.

5. Oxide removal for NPN emitter and N channel source and
   drain (Mask No. 3).

6. N+ type diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

The epitaxial diffused approach is shown in Figure 47. This approach
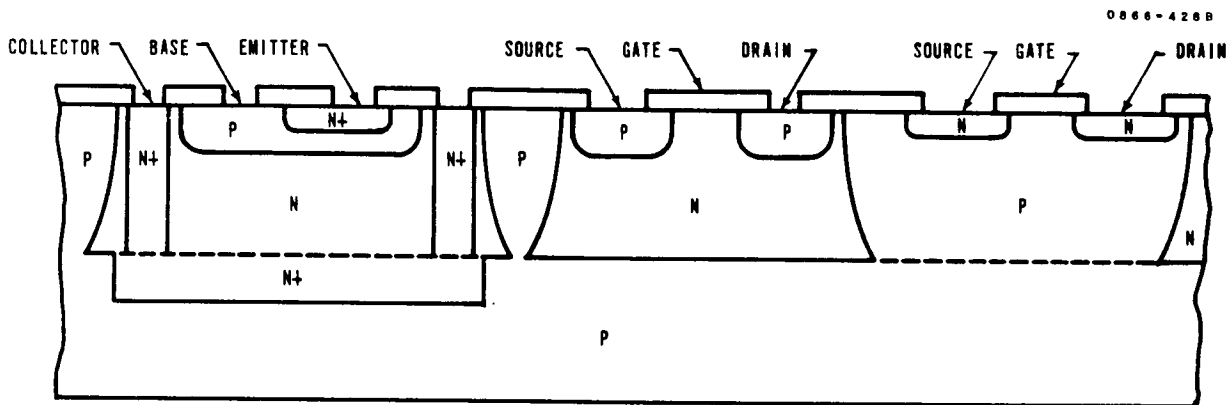

FIGURE 47. SKETCH OF COMPLEMENTARY MOSTs AND
A HIGH CURRENT NPN BIPOLAR TRANSISTOR IN
THE SAME CHIP CONSTRUCTED OF EPITAXIAL MATERIAL

provides a function with the capability of higher operating speeds, lower
power dissipation, and higher current NPNs than the all-diffused approach.
The process utilizes a P type substrate with an epitaxially grown N type
layer. An N+ buried layer and a deep N+ diffusion is used to reduce the
saturation resistance of the NPN. The process steps required for the
fabrication of this device are (starting with the P type substrate):

1.   Remove oxide in N+ buried layer regions (Mask No. 1).

2.   Diffuse N+ buried layer.

3.   Grow N type epitaxial layer.

4.   Grow oxide over entire surface.

5.   Remove oxide for isolation regions (Mask No. 2).

6.   P type isolation diffusion.

7.   Remove NPN collector contact oxide (Mask No. 3).

8.   Deep N+ diffusion.

9. Remove oxide for P channel source and drain, and NPN base (Mask No. 4).

10. P type source, drain, and NPN base diffusion.

11. Remove oxide for N channel source and drain, NPN emitter, and NPN collector contacts (Mask No. 5).

12. N+ type diffusion.

13. Gate oxide formation (Mask No. 6).

14. Contact oxide removal (Mask No. 7).

15. Metallization (Mask No. 8).

The parameters of each component can be improved at the expense of additional process steps in the formation of the channels, gate oxide, and the metallization. The fabrication of the above device presents a very difficult task in the area of process control, but the end result is a very efficient circuit.

The use of epitaxial material in the fabrication of any of the previous devices will result in considerable improvement in device parameters.

9.2 PLATED WIRE MANUFACTURING PROCESS

A flow chart of a plated wire manufacturing process is shown in Figure 48. The steps listed show a representative process, which is only one of numerous processes which can be utilized. A photograph of the Aero-Florida magnetic wire plater is shown in Figure 49.

The plating process begins with a spool of beryllium-copper (Be-Cu) wire 5 mils in diameter. The wire moves continuously through each process step and is cut into definite lengths after the final on-line anneal step.

The wire first goes through several surface conditioning and cleaning steps prior to receiving an electrodeposited film of pure copper. The wire is now ready for the plating of the magnetic film. This is accomplished by a Honeywell developed process which precisely controls the materials composition, rate of deposition, film thickness, and magnetic properties.
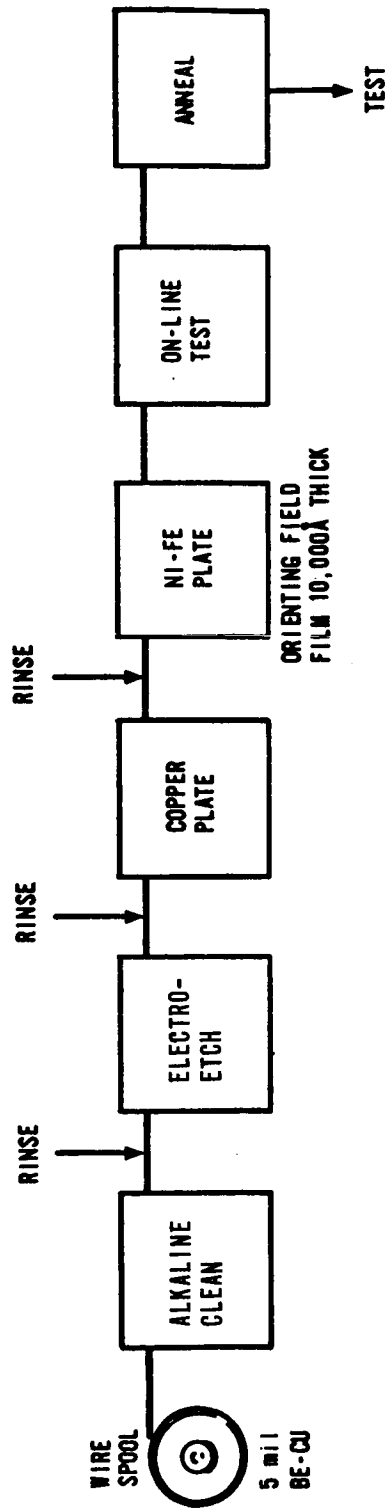
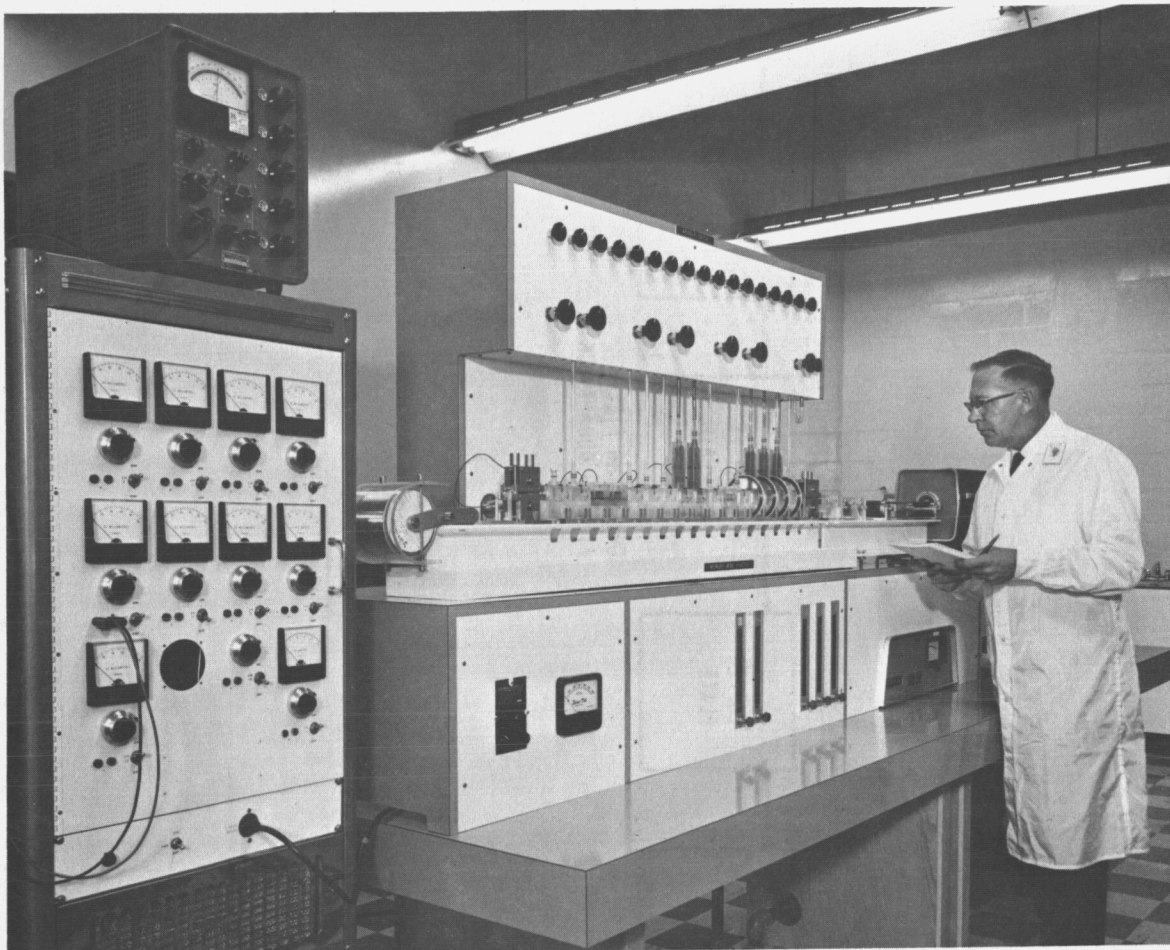FIGURE 48.   MAGNETIC FILM PLATER OPERATIONAL BLOCK DIAGRAM

A6610-39

FIGURE 49.   MAGNETIC THIN FILM WIRE PLATER

Within the plating system, provisions are made for continuous testing of the magnetic properties. These tests include measurement of H_c (coercive force), H_k (anistropy constant), dispersion, and skew.

Honeywell can also perform pulse tests for storing information, digit disturb, and nondestructive readout level in an on-line tester which is part of the plating system. Post deposition anneal is performed after plating and initial test.

An off-line tester, Figure 50, consists of high quality commercial laboratory equipment for pulse testing the wire and selection of wire which meets the necessary parameters to satisfy the memory system requirements such as creep, digit disturb levels and specified output voltage.

Honeywell has developed a technique to measure the switching astroid of the plated wire. This test is significant in determining the NDRO capability of the wire. Honeywell designed instrumentation is used to perform the test.

A test facility, Figure 51, is available for measurement of H_c, H_k, skew and dispersion as a function of amount of stress and degree of twist. This test is also utilized as a measurement of the composition of the magnetic alloy.

An apparatus which facilitates the study of aging of plated wire has been developed by Honeywell. This equipment applies a temperature gradient to the wire for the purpose of accelerating any aging effects. This provides information applicable to the anneal cycle which assists in the prevention of aging problems in plated wire memory systems.

Upon completion of the off-line test program, the plated wire is ready for assembly into a memory plane and further testing as a complete sub-assembly.
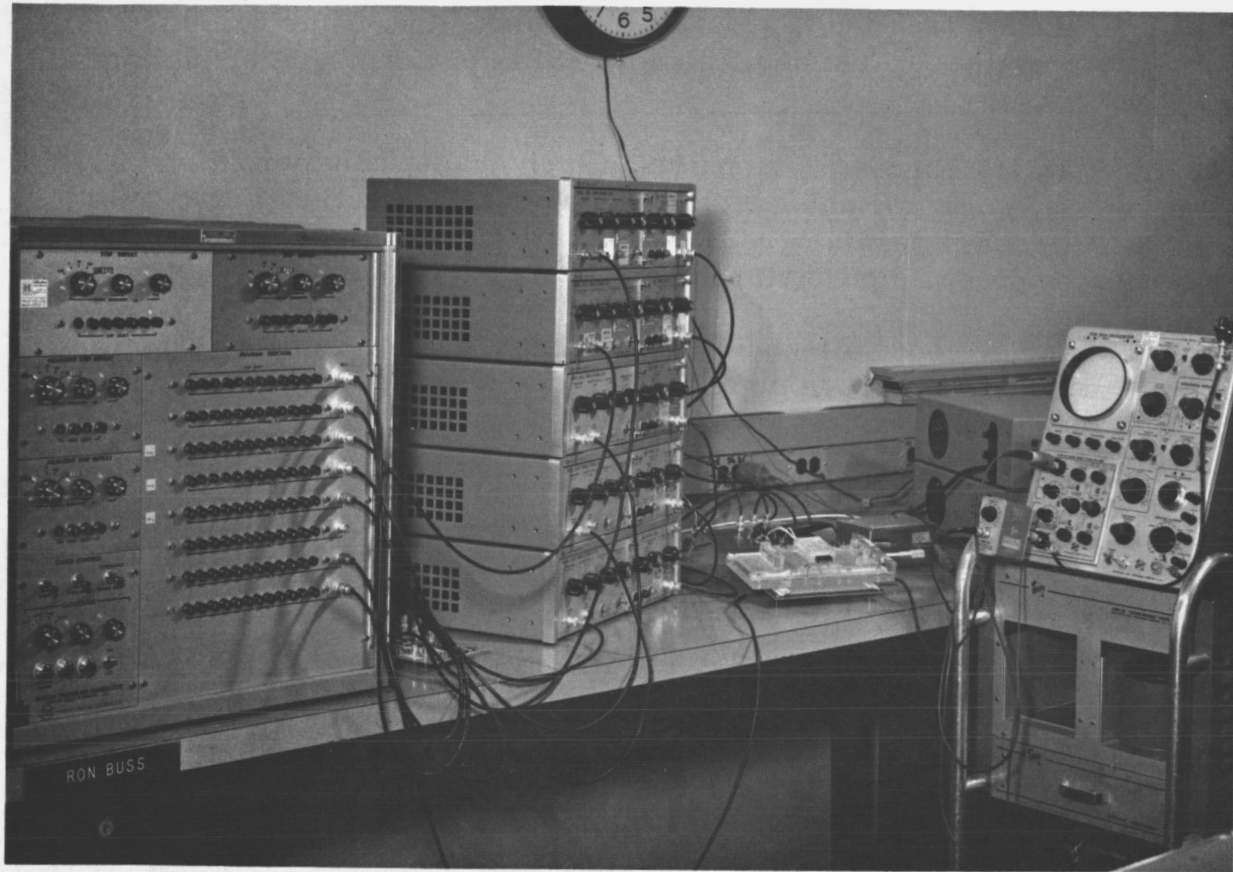
A6604-129
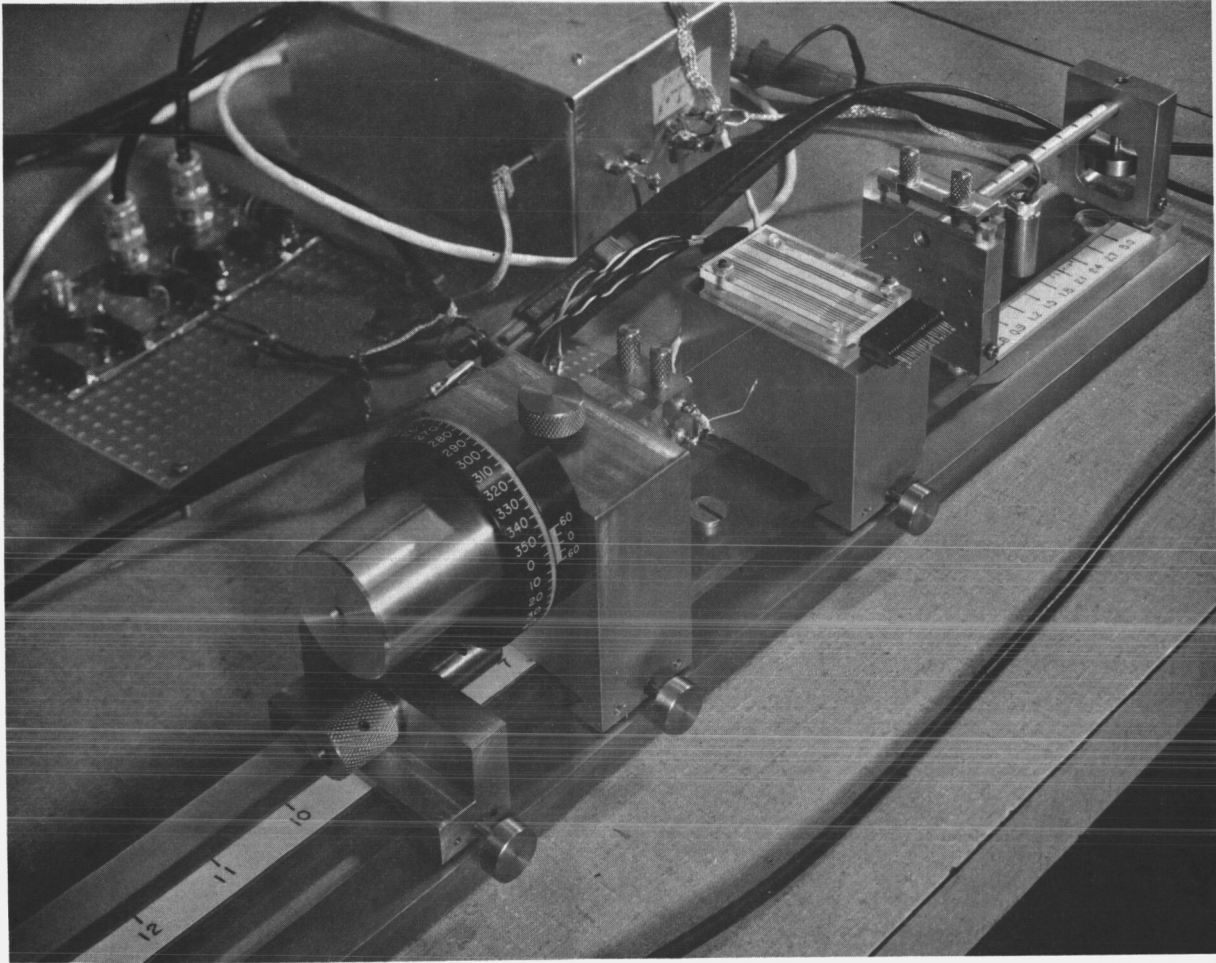

FIGURE 50.   PULSE TEST EQUIPMENT

A6607-040

FIGURE 51.   TORSIONAL STRAIN - SKEW EQUIPMENT

10.0 POWER AND SPEED REQUIREMENTS

10.1 MEMORY CYCLE TIME

The cycle time of an MOS plated wire memory is determined by the total time required to address a word and receive the stored information as a logic output. The total time for one complete memory cycle is equal to the sum of the following: clock pulse width (t_{cw}), settling time of the address register (t_{ad}), delay time of the address decoding logic (t_{dl}), rise time of word drive selection (t_{ws}), rise time of word current (t_{wc}), delay time of sense line (t_{sl}), delay time of the sense amplifier (t_{sa}) and settling time of the information register (t_{ir}). Hence

$$t_{cy} = t_{cw} + t_{ad} + t_{dl} + t_{ws} + t_{wc} + t_{sl} + t_{sa} + t_{ir}$$

The address decoding network shown in Figure 52 will be used in calculating the delay time. The delay time associated with MOS circuitry is RC limited. The load MOST, Q_5, has a R_{on} of 25K ohms while the gate MOSTs, Q_1 through Q_4, have a R_{on} of 2.5K ohms.

The output capacitance of the decoding gate is expressed as:

$$C_o = C_{DS(1-4)} + C_{im} + C_{in-6}$$

where

$C_{DS(1-4)}$ is the sum of the drain to source capacitance of Q_1 through Q_4

C_{im} is the interconnection metalization capacitance between the decoding gate and the input of Q_6

C_{in-6} is the gate input capacitance of Q_6

also,

C_{DS} is a p-n junction capacitance of approximately 0.1 pf/mil^2

C_{im} is a thick oxide capacitance of approximately 0.03 pf/mil^2

C_{in} is primarily a thin oxide capacitance of approximately 0.25 pf/mil^2

1066-340A

FIGURE 52.   SCHEMATIC DIAGRAM OF AN ADDRESS
DECODING NETWORK

Using these values, C_o becomes

$$C_o = (2.1 + 0.1 + 0.2) \text{ pf} = 2.4 \text{ pf}$$

Assuming three time constants for turn off time of the decoding logic t_{dl} becomes

$$t_{dl} = 3 R_{on} C_o = (3)(25 \times 10^3)(2.4 \times 10^{-12})$$

$$= 180 \text{ nanoseconds}$$

In a similar manner, the remaining delay times can be calculated. For a 1,000 word memory, the total cycle time for READ ONLY becomes:

$$t_{cy} = t_{cw} + t_{ad} + t_{dl} + t_{ws} + t_{wc} + t_{sl} + t_{sa} + t_{ir}$$

$$= \left[(500) + (800) + (180) + (300) + (50) + (10) + (100) + (600) \right] \text{ nanoseconds}$$

$$\cong 2.6 \text{ microseconds}$$

A 1,024 word 26-bit memory operating in a READ ONLY mode at a 2.6 microsecond cycle time would have a total power dissipation of approximately 45 watts. Both cycle time and power dissipation can be improved considerably by the use of complementary MOS devices. Complementary devices are discussed in the following paragraphs.

## 10.2 COMPLEMENTARY MOST LOGIC CIRCUITS

The most significant features of complementary MOST circuitry are:

Higher Switching Speeds

Lower Power Dissipation.

These can be discussed further by the examination of Figure 53. The use of a single type MOST, P channel in this case, for both the active device and the load resistor is shown in 53a. Complementary P channel and N channel MOSTs are illustrated in 53b.

The operation of the inverter circuit in Figure 53a is as follows. The input voltage swing is from near ground to a voltage near $-V_{DD}$. When

1066-339A
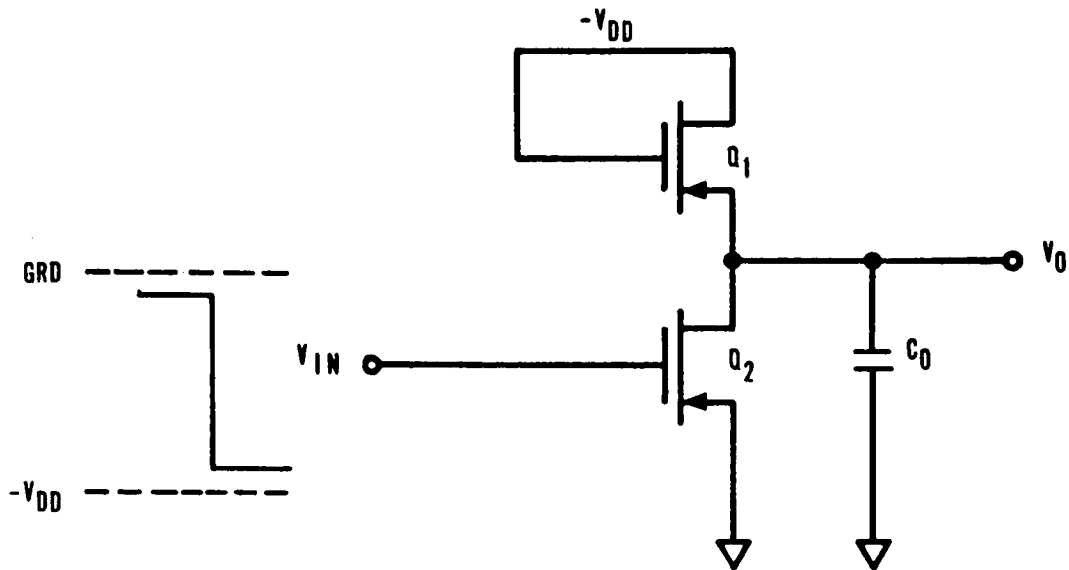
a. Inverter circuit using P channel MOSTs as both the active
device and the load resistor.
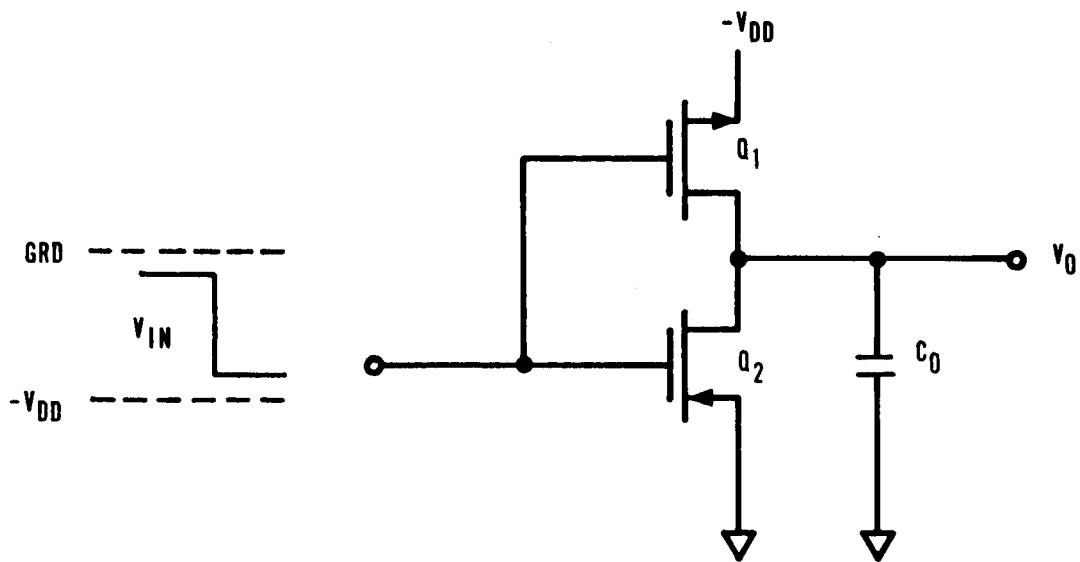
b. Inverter circuit using P channel MOST as the active device
and an N channel MOST as the load resistor.

FIGURE 53. MOST INVERTER CIRCUIT CONSTRUCTED AS
(a) SINGLE TYPE MOSTs (b) COMPLEMENTARY MOSTs

the input is near ground the V_{GS} of Q_2 is below its threshold and Q_2 is off. The output then is more positive than the supply voltage by the magnitude of the threshold voltage of Q_1:

$$V_o = -V_{DD} + V_T$$

When the input is near the supply voltage, the threshold voltage of Q_2 is exceeded and it is turned on. The output voltage becomes equal to:

$$V_o = \frac{R_{on\,2}(-V_{DD})}{R_{on\,1} + R_{on\,2}}$$

The manner in which Q_1 is connected dictates that it is always turned on and, in this case, both Q_1 and Q_2 are on. The output voltage is a result of the resistor divider action of the "on" resistance of the two MOSTs. This means that the R_{on} of Q_1 should be approximately equal to $10 \times R_{on}$ of Q_2 in order for V_o to be near ground. The resulting switching time will be a function of the output $R_{on} C_o$ time constant during turn-on and turn-off of Q_2. (C_o is defined as the total output capacitance loading the inverter.) The rise time during turn-off will be approximately ten times greater than the fall time during turn-on. The overall propagation delay time through a logic network is therefore limited by the "on" resistance of the load MOST. Power dissipation for a large network can become excessive as a consequence of both Q_1 and Q_2 being on at the same time.

The use of complementary MOSTs as shown in Figure 53b solves both of the above problems. With an N channel MOST as the load and a P channel MOST as the active device, the inverter circuit operates as follows. When the input voltage is near ground Q_2 is off and Q_1 is on. The output capacitance, C_o, charges through the "on" resistance of Q_1 with a time constant of $R_{on1} C_o$. During quiescent conditions either Q_1 or Q_2 is off, and this presents a very high resistance between the supply voltage and ground. The only current present is the leakage current of the drain junction. Both Q_1 and Q_2 must be enhancement mode devices in order for the input voltage to turn one or the other completely off. The gate of Q_1 is always more positive than its source and the gate of Q_2 is always more negative than its source, hence only enhancement mode devices will provide the required turn-off action. The "on" resistance of Q_1 and Q_2 can be made equal and as low as practical, hence the turn-on and turn-off times will be symmetrical. The total propagation delay time of a complete logic network will be approximately an order of magnitude less than for the single type MOSTs discussed previously. Since one of the MOSTs is normally off the stand-by power dissipation is reduced to a minimum. The total power dissipation becomes

a function of the repetition rate and the magnitude of C_o, because most of the power is used in charging and discharging this capacitance. It can be shown that the total power dissipation is equal to:

$$P_d = C_o V_{DD}^2 f + P_s$$

Where C_o if the total output capacitance. V_{DD} is the supply voltage f is the repetition rate and P_s is the standby power (P_d was incorrectly given in the 5th report as $P_d = 2 C_o V_{DD}^2 f + P_s$). Power dissipation as a function of clock rate is illustrated by the curve shown in Figure 54. This curve indicates that complementary MOS devices are ideal for spacecraft systems where clock rates vary considerably as a function of each phase of the mission.

Therefore the use of complementary MOSTs for logic circuits offers a significant increase in speed and a considerable reduction of power dissipation. The mechanization of both a NAND gate and a NOR gate is shown in Figure 55.

In Section 6 complementary MOSTs were shown to reduce the delay time through the word driver circuit from 300 nanoseconds to 100 nanoseconds.
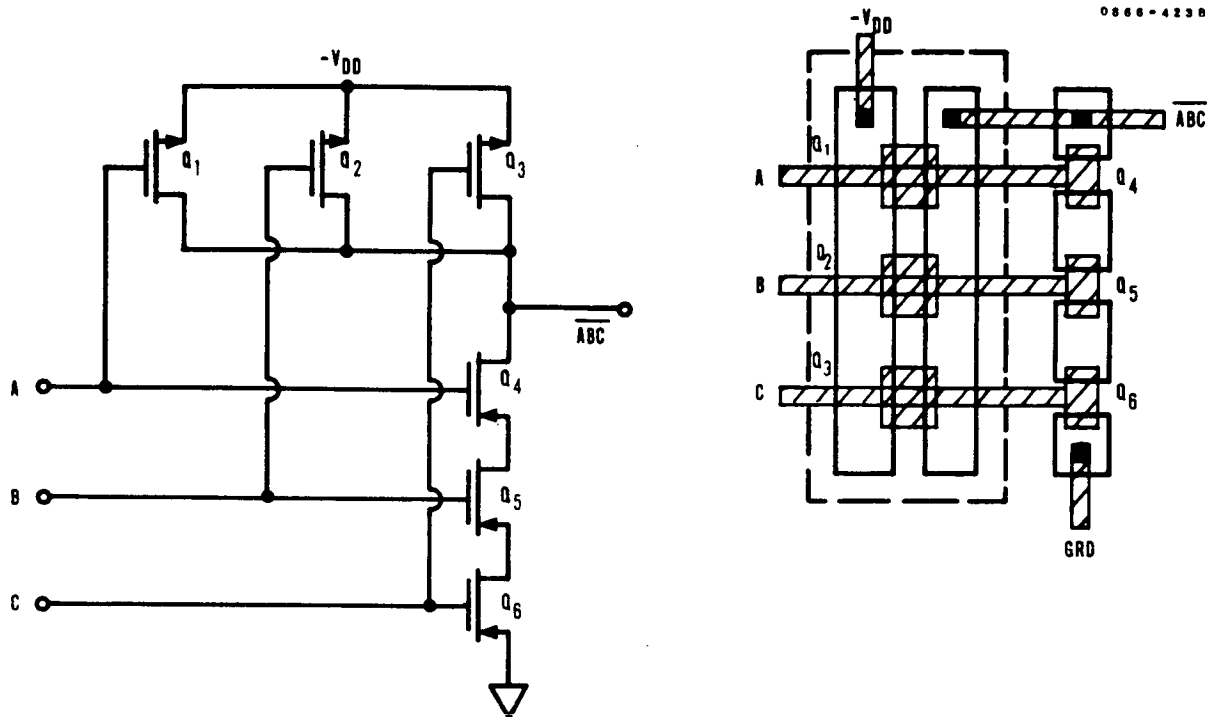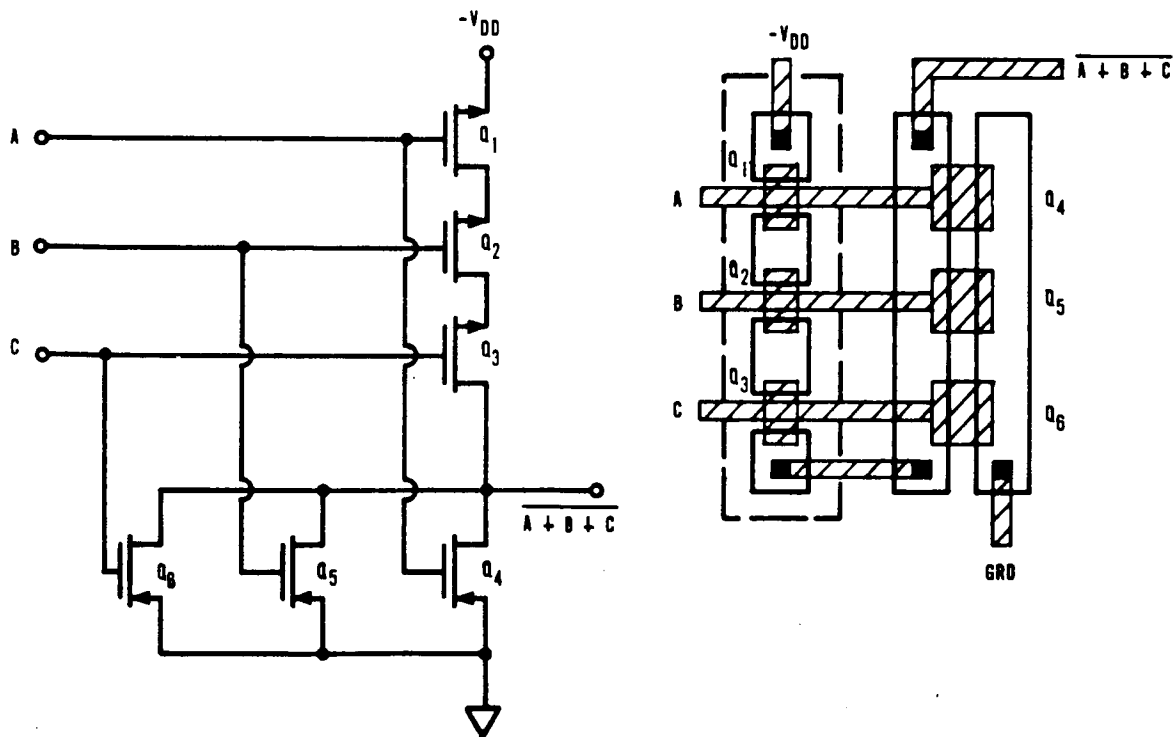
1066-342A
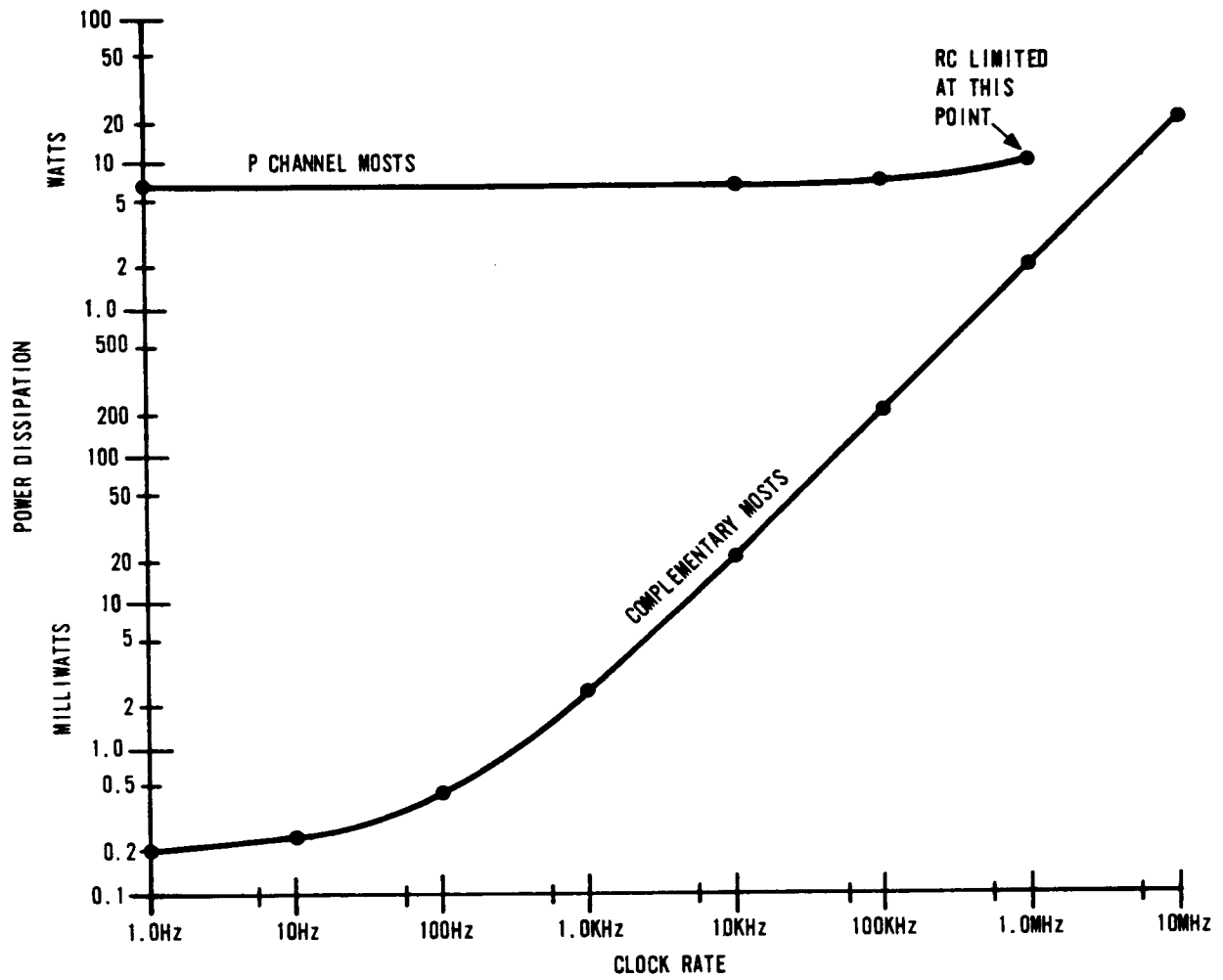
FIGURE 54. COMPLEMENTARY MOST LOGIC POWER DISSIPATION AS A FUNCTION OF CLOCK RATE FOR A 1,000-CIRCUIT SYSTEM

(a) Complementary MOST NAND gate circuit and chip layout.

(b) Complementary MOST NOR gate circuit and chip layout.

FIGURE 55. COMPLEMENTARY N AND P CHANNEL MOST LOGIC MECHANIZATION

11.0 FEASIBILITY BREADBOARD MEMORY SYSTEM

A plated wire memory system was fabricated, using MOS transistors and integrated circuits for the electronics, to illustrate the use of MOS devices for interfacing directly with plated wire memory elements. The breadboard system included a 16 word, 2 bit memory plane; selection circuitry, word drivers, sense amplifiers, timing and control, and the required switches and indicators for exercising and operating the memory system. As will be discussed, the word drivers and sense amplifiers proved to be the most difficult applications for MOS transistors, but they were still able to perform the required function.

The memory system was designed for a READ cycle time of 10 microseconds (100 kc Clock Rate) and the system operated well within this limit. Two external power supplies are required for system operation: +20 volts dc at 0.25 amps maximum and -25 volts dc at 1.3 amps maximum. Two other voltages, -20 volts dc and -15 volts dc, are required internally but these are generated from the -25 volts dc supply by using Zener diode regulators. Protection circuitry is provided for protection against excessive and/or reverse polarity supply voltages. A combination of a Zener diode and a high current SCR is used to protect against excessive supply voltage. An overvoltage causes the Zener to conduct, hence firing the SCR which clamps the power bus to ground. This causes excessive current to flow which blows the power supply fuse or circuit breaker. High current diodes are placed across the power bus to protect against a reverse polarity voltage.

The completed system is shown in Figures 56 and 57.
Figure 56 is a photograph of the system cabinet and operator's panel. Figure 57 is a photograph of the internal assembly which shows the memory plane, circuit breadboards, and power controls. A photograph of the memory plane is shown in Figure 58. The plated wire used in this memory plane was fabricated by an in-house plating system.

The operating procedures for the feasibility breadboard memory system are outlined completely in Appendix A.

11.1 BREADBOARD CIRCUITRY

A functional block diagram of the complete memory system is shown in Figure 59. The circuit section of the system consists of the selection, sense amplifier, and timing and control circuitry. These are discussed in the following paragraphs.

Word Selection Circuitry

The complete word selection circuitry consists of the address register, the decoding logic, and the word drivers. The schematic diagram of the word selection circuitry is shown in Figure 60. The address register is a conventional four stage binary counter constructed of MOS flip-flops (type number MEM 1005) and MOS three input gates (type MEM 1002). Both of these devices are monolithic integrated circuits available from General Instrument Corporation, and copies of the manufacturer's specification sheets are included in Appendix B. A photograph of the address register board is shown in Figure 61. The decoding logic was mechanized with the MEM 1002 three input gate. A photograph of the decoding board is shown in Figure 62. The word driver consists of a predriver stage which uses two General Instrument type MEM 517A MOS transistors and a final output driver using one MEM 517A. The predriver also provides a gating function which gates the READ pulse into the selected word driver. Both the predriver and the driver are operated with a supply voltage of -25 volts in order to obtain 400 ma from a single MEM 517A. The output word driver is connected to -25 volts dc at the plated wire memory plane. A photograph of the word driver board is shown in Figure 63.

Sense Amplifier

The complete sense amplifier consists of two differential amplifier stages, two single ended amplifier stages and an output latch. The schematic diagram of the sense amplifier is shown in Figure 65. The differential amplifiers consist of matched pairs of 3N128 MOS high frequency transistors and selected resistor values in order to obtain the necessary common mode rejection. Capacitive coupling is used throughout to alleviate the drift problem. Source followers are used between each stage of amplification in order to obtain the required high frequency gain. The complete amplifier has an overall voltage gain of 2,000 and a common mode rejection ratio of 1,000 to 1 at 10 mc. The latch is constructed with Fairchild 2N4067 and General Instruments 2N4353 MOS transistors. Copies of the manufacturer's specification sheets are included in Appendix B.

Included as part of the sense amplifier section is the bit-write circuit. This circuit provides a dc current of 35 ma during the write mode of operation. A photograph of the sense amplifier board is shown in Figure 64.

11.2 TIMING AND CONTROL

The timing and control circuitry consists of an astable multivibrator and a number of monostable multivibrators (one-shots) which provide the necessary time delays and pulses for proper system operation. A schematic diagram of the timing and control circuitry is shown in Figure 66. The astable multivibrator operates at 100 kHz in the free-running mode, but in the one-shot mode a single pulse is provided each time the push-button switch (S3) is depressed. The RUN/START-STOP switch (S1) is used to shock the astable multivibrator into oscillation when power is first turned on and when the operating mode is changed from one-shot to 100 kHz.

Extensive use is made of complementary MOS transistor inverters as buffer amplifiers for obtaining fast rise and fall times without excessive power dissipation. The complementary inverters use the Motorola 2N4351 N channel enhancement mode MOST as the load resistor and either the General Instrument 2N4353, MEM 517A, or MEM 520 P channel MOST as the active element.

The timing and control outputs consist of: address clock, data register reset, read pulse, strobe delay, and strobe. The timing diagram for both the READ mode and WRITE mode is shown in Figure 67. The address register is set up on the leading edge of the clock. The data register is reset on the trailing edge. After a 1.3 microsecond delay from the trailing edge a 0.5 microsecond READ pulse is generated. An 80 nano-second strobe pulse is delayed 80 nanoseconds from the leading edge of the READ pulse and is used to gate the sense amplifier output into the data register. A composite photograph of the 16 word currents and sense amplifier outputs (inputs to data register) is shown in Figure 68. The same sequence of pulses occurs during the WRITE mode along with a dc bit current which is utilized to store the information on the plated wire. A more detailed outline of the system operation is included in Appendix A.

A photograph of the timing and control circuit board is shown in Figure 69.
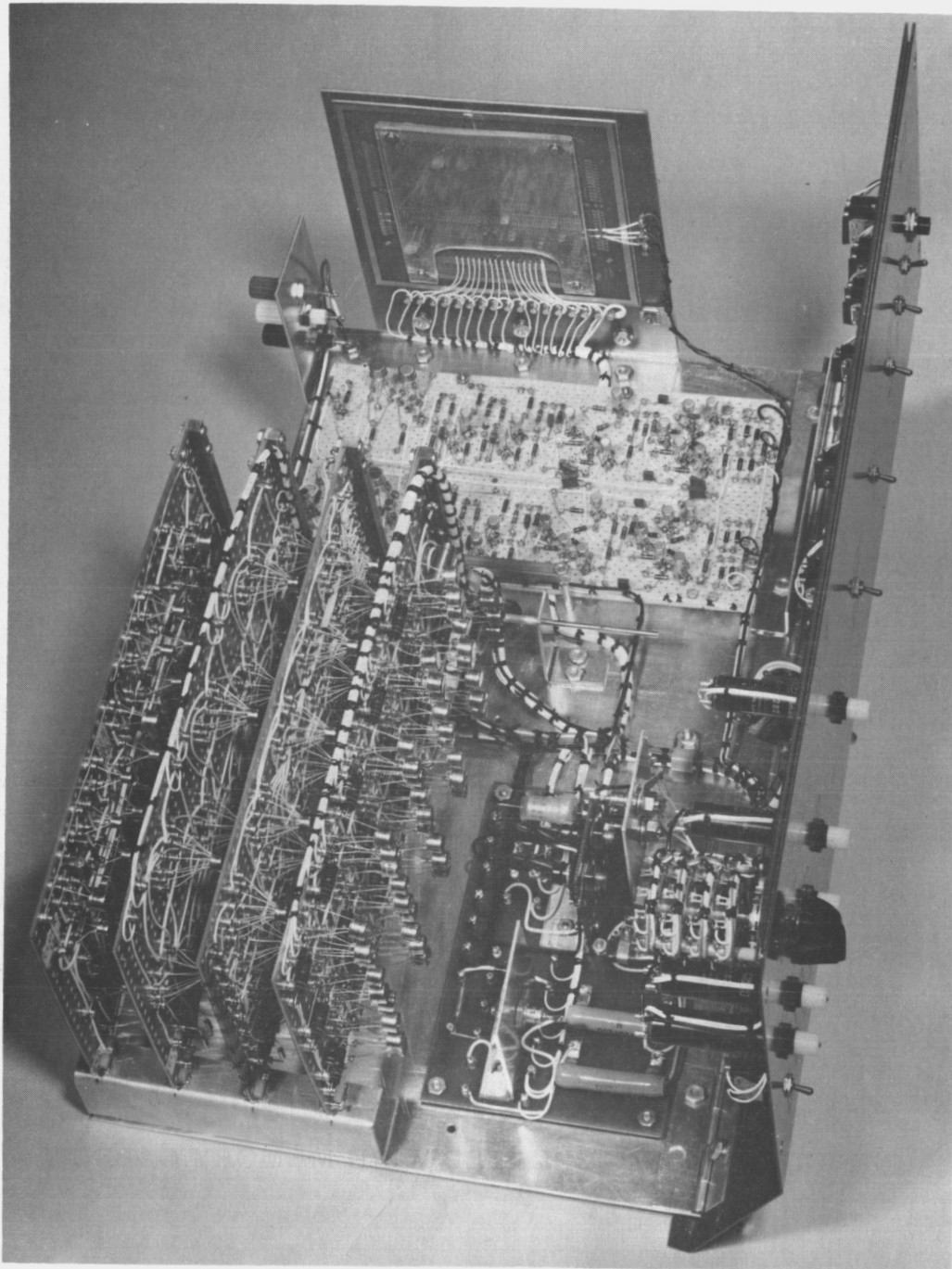
A6701-54

FIGURE 56. MOS PLATED WIRE MEMORY CABINET
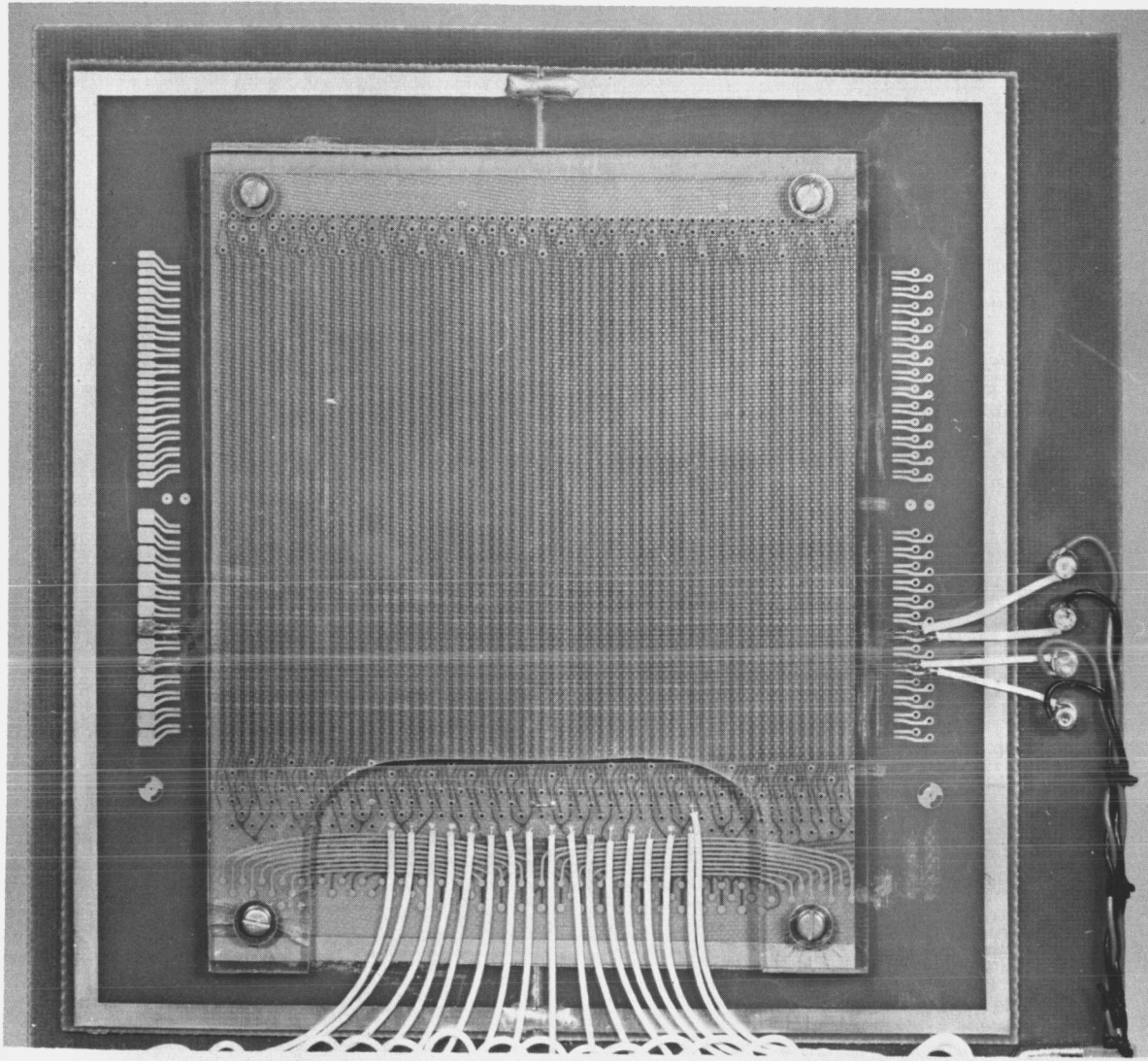
A6701-58-1

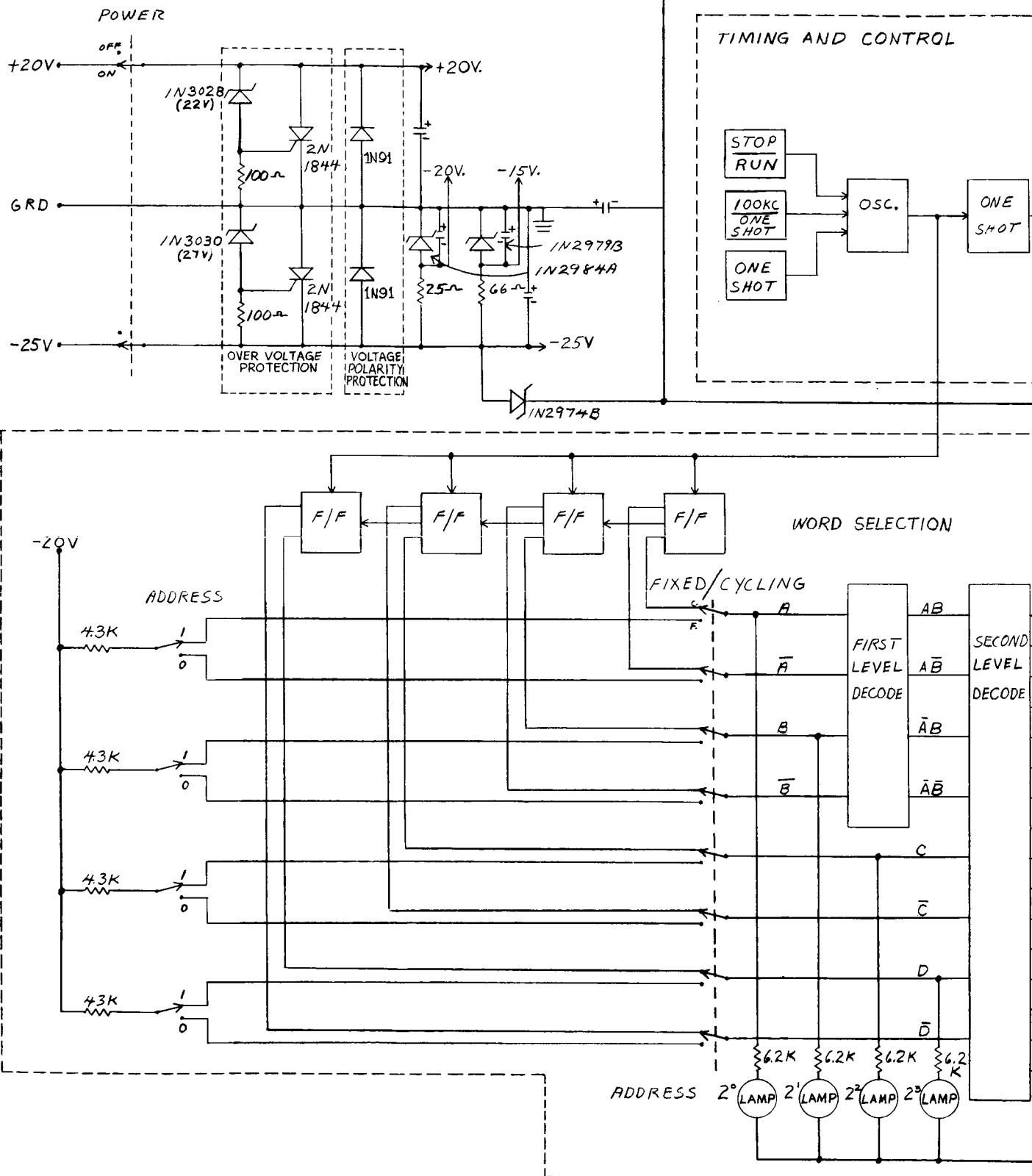FIGURE 57. MOS PLATED WIRE MEMORY SYSTEM ASSEMBLY

A6701-61

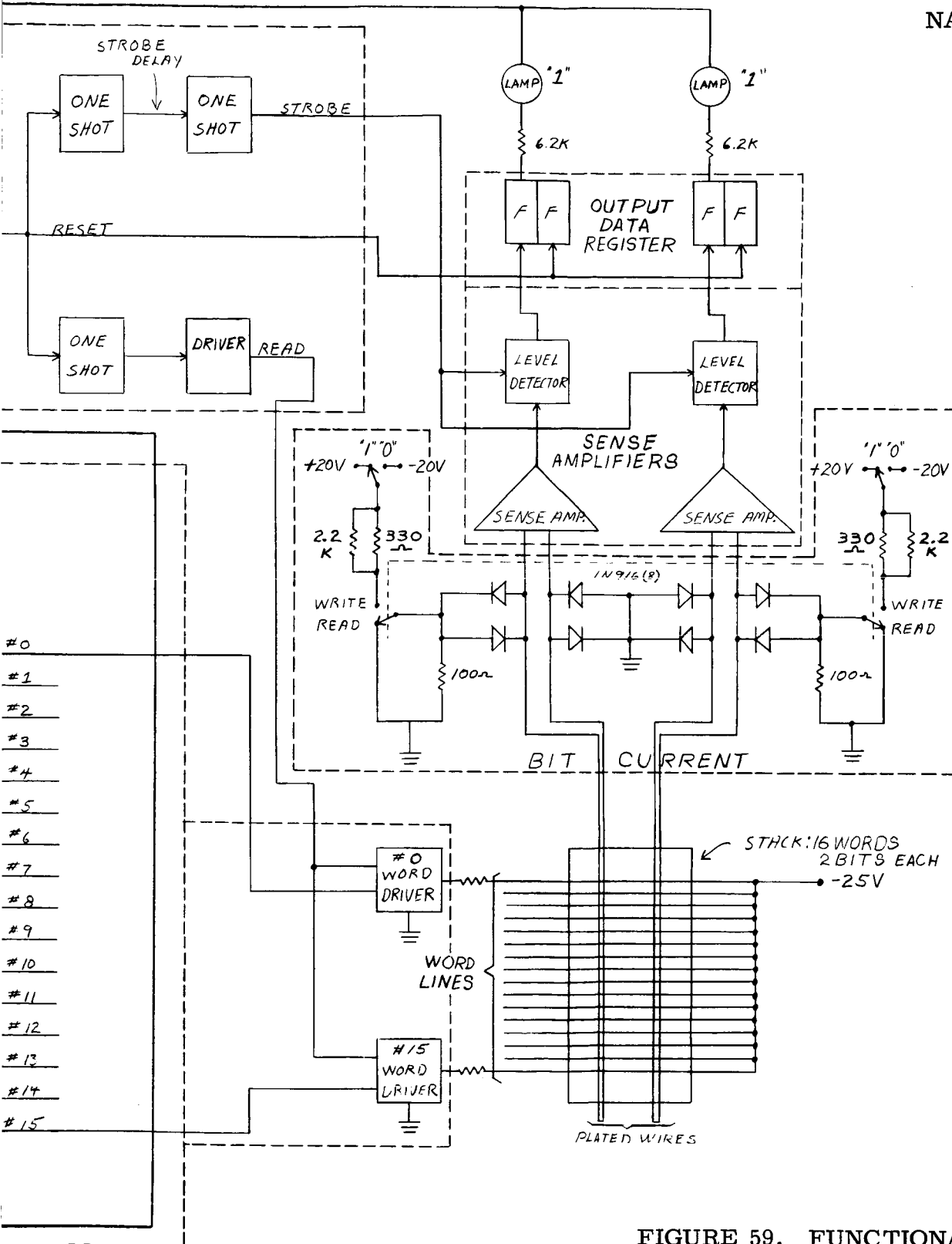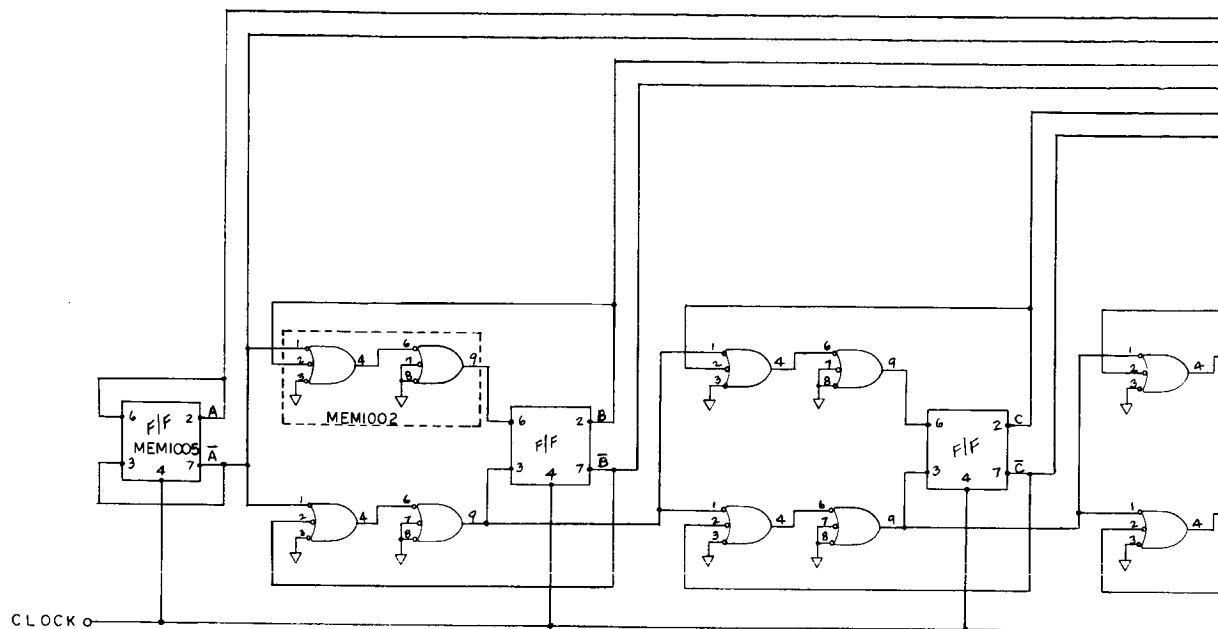FIGURE 58.   PLATED WIRE MEMORY PLANE

FIGURE 59. FUNCTIONAL BLOCK
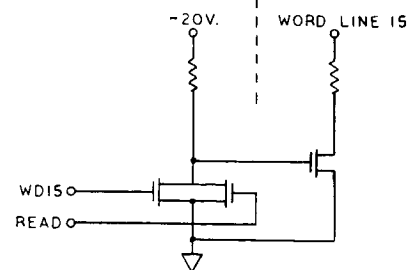DIAGRAM OF MOS PLATED
WIRE MEMORY SYSTEM

CLOCK

LOGIC "1"= 0 V.

LOGIC "0"= - V.

-20V.   WORD LINE 0

680 Ω
(16)

R_SEL
(16)

Q1   Q2   Q3

WD0

READ
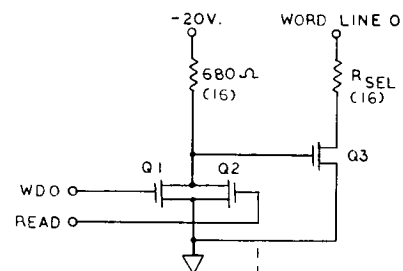
Q1 Q3   MEM517A
Q2   MEM517

-20V.   WORD LINE 15

WD15

READ
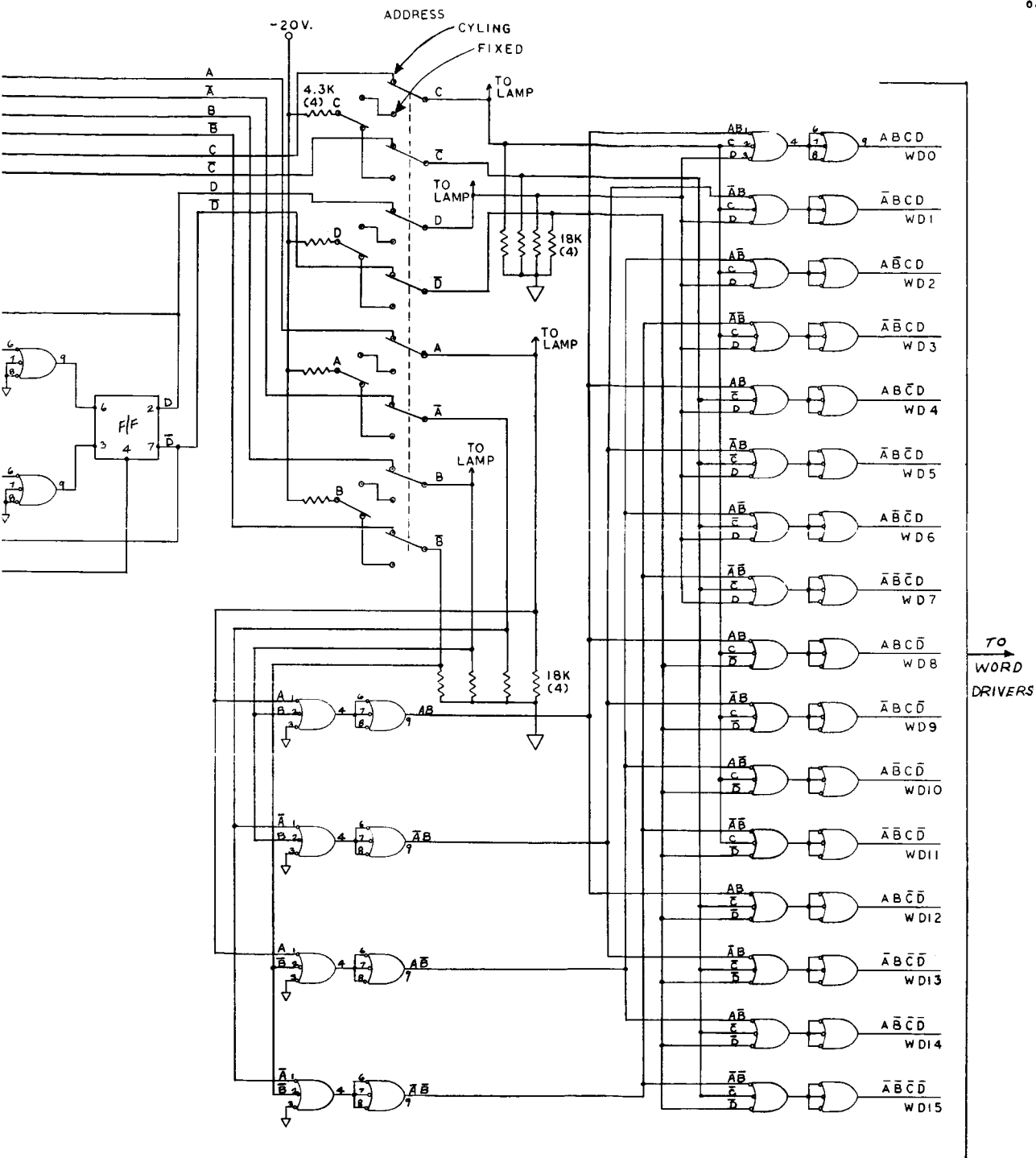
WORD DRIVER

FIGURE 60. SCHEMATIC DIAGRAM
OF THE WORD SELECTION CIRCUIT
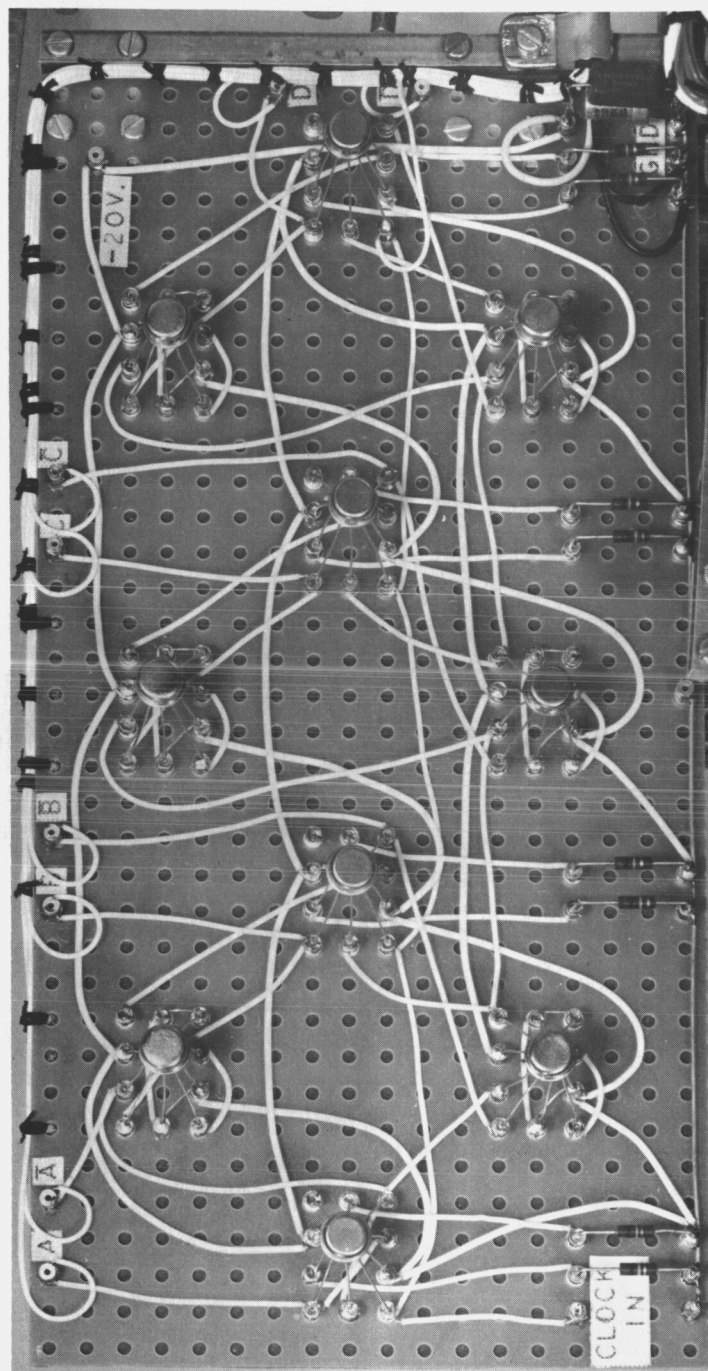
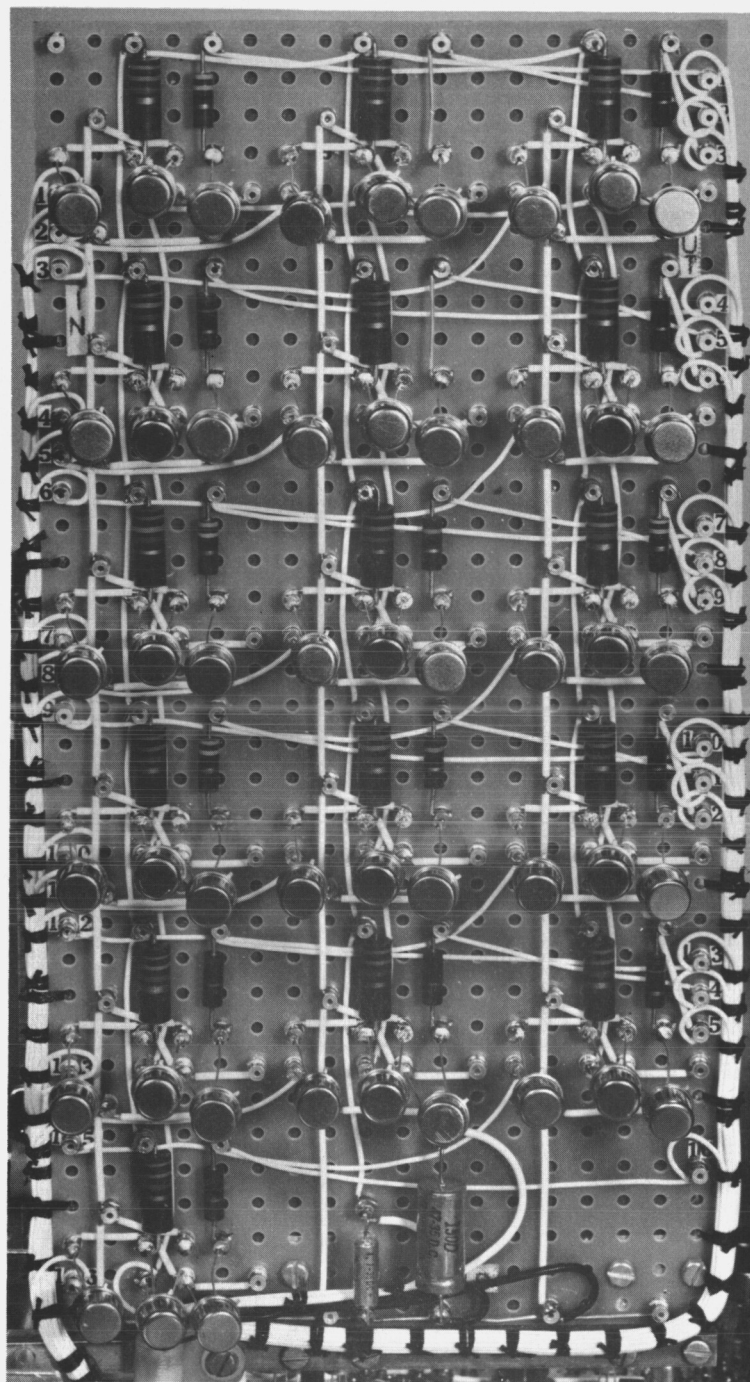FIGURE 61.   ADDRESS REGISTER BOARD
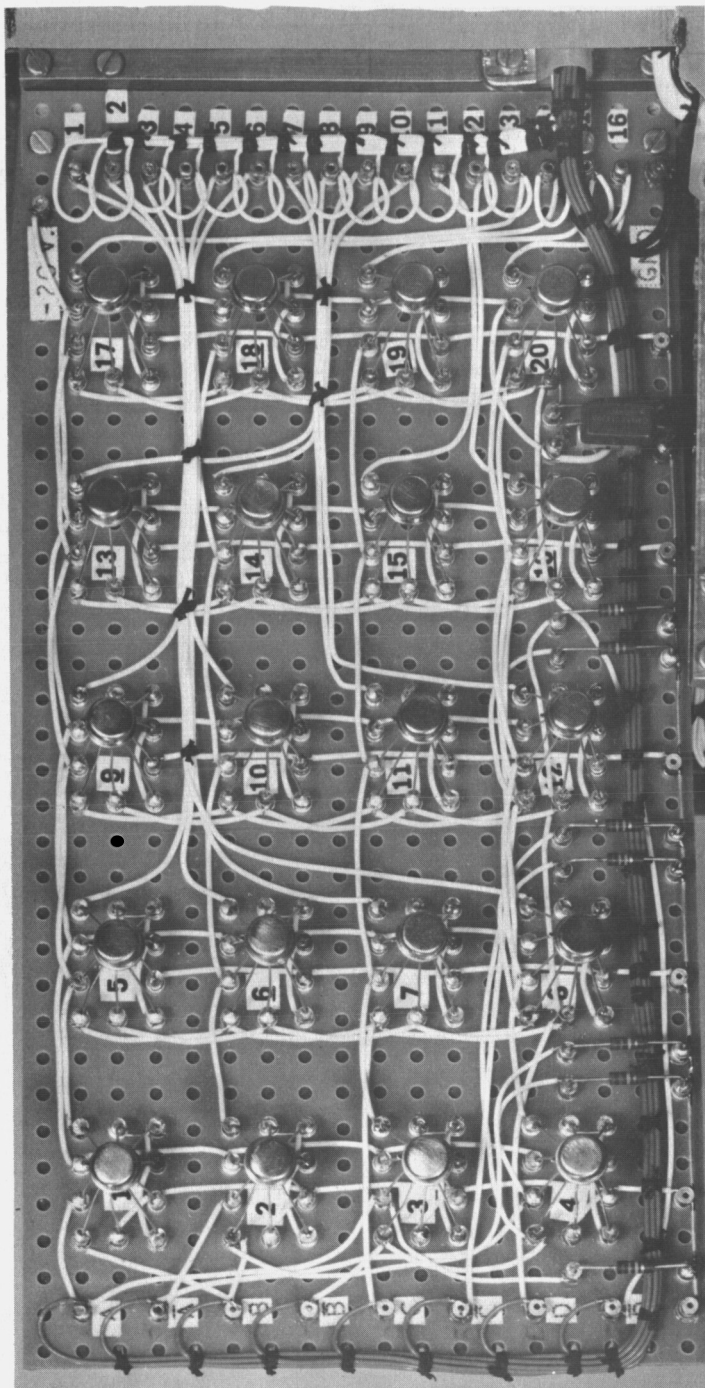
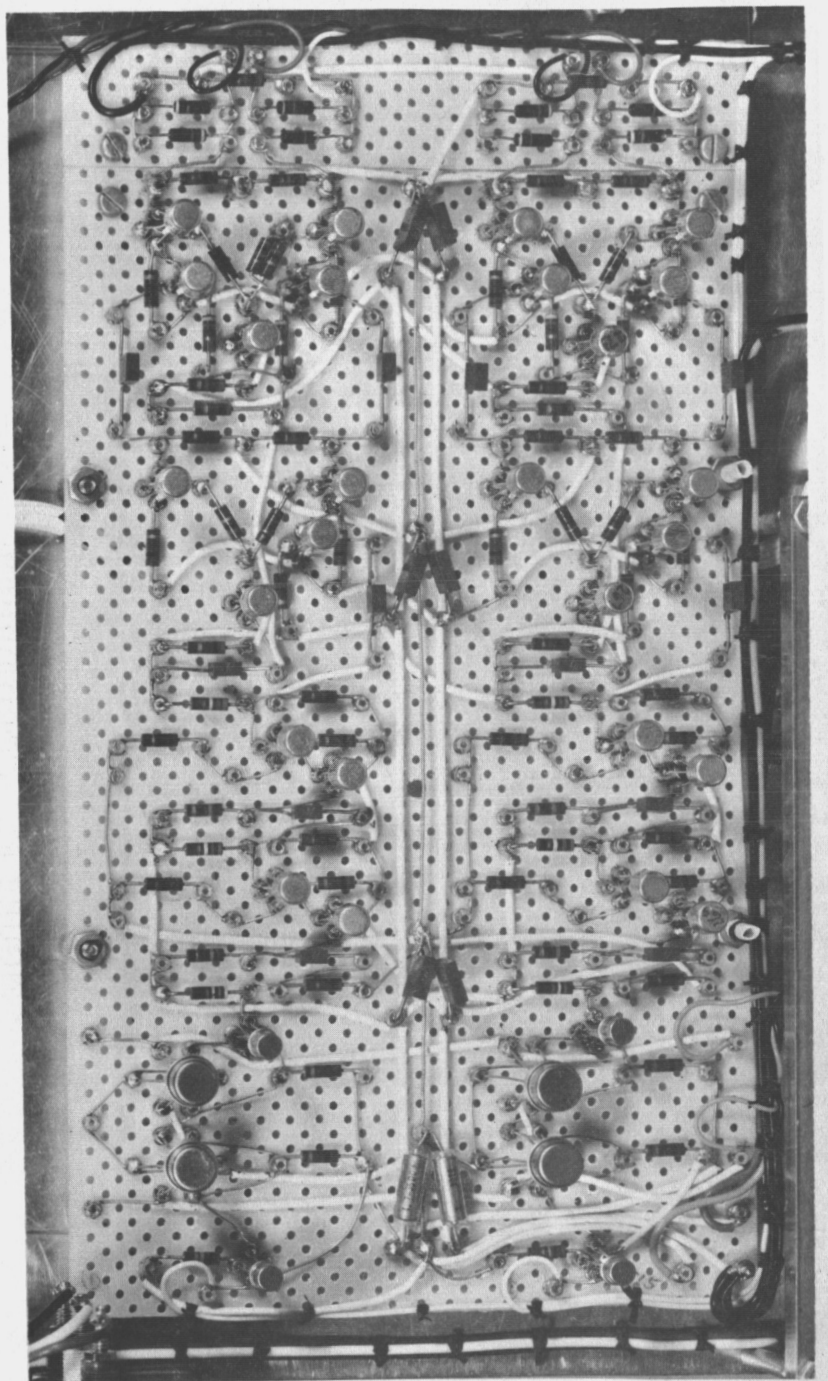FIGURE 62. ADDRESS DECODING BOARD

A6701-63

FIGURE 63. WORD DRIVER BOARD

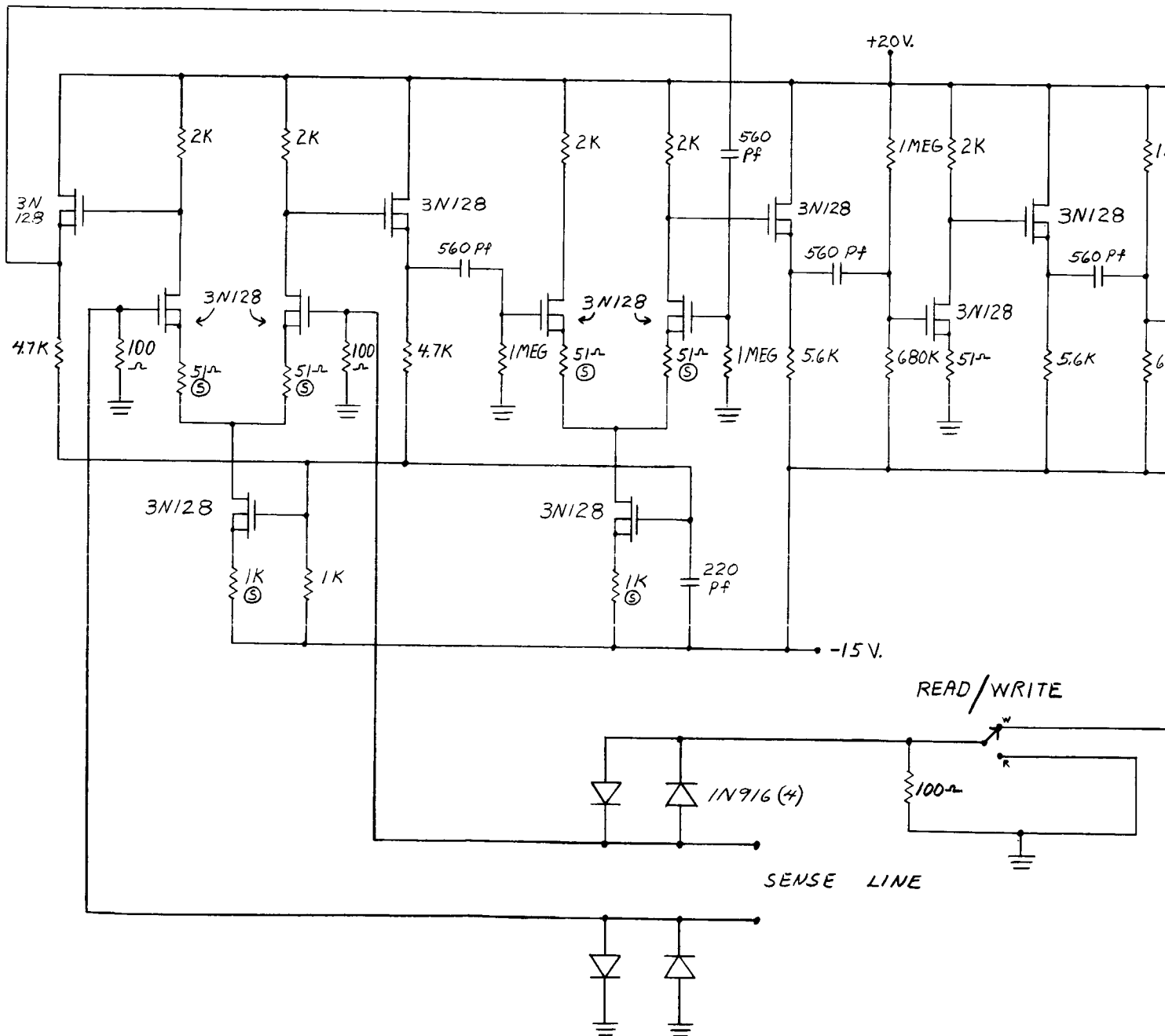FIGURE 64. SENSE AMPLIFIER BOARD

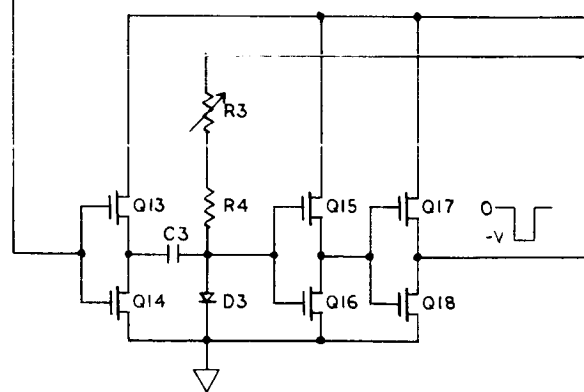(S) — SELECTED RESISTOR

109

FIGURE 65.   SCHEMATIC DIAGRAM
OF THE MOS TRANSISTORIZED
AMPLIFIER

OSCILLATOR
100 KHZ

DELAY AND RESET
1.3 μ SEC.

TO
ADDRESS
REGISTER

Q25 Q27 Q29

Q26 C8 C9 Q28 Q30

D5 R6 R7 D6

CLOCK

Q1 C1 R1 Q3 Q5

Q2 D1 Q4 Q6

STROBE DELAY
80 N. SEC.

PRESS TO
ONE SHOT

100KHZ

S2
ONE SHOT S3 PB

O - 20 V.

R3

RUN

S1

STOP
START

Q13 R4 Q15 Q17

C3

Q14 D3 Q16 Q18

FRONT PANEL

0467-117N

READ
.5 μ SEC.

INVERTER

-20V.

+20V.

Q7 R2 C2 Q9 Q11 O -V

Q8 D2 Q10 Q12

R8
-V
O READ
Q31

O RESET
(DATA REGISTER)

STROBE
80 N. SEC.

+C5

+C6

Q19 R5 C4 Q21 Q23 O -v

Q20 D4 Q22 Q24

O STROBE

C1	2200 PF
C2	470 PF
C3	200 PF
C4	270 PF
C5 C6	4.7 MF
D1 D2 D3 D4 D5 D6	1N916
Q1 Q3 Q5 Q7 Q9 Q11 Q13 Q15 Q17 Q19 Q21 Q23	2N4351
Q2 Q8 Q14 Q20 Q31	MEM517A
Q4 Q6 Q10 Q12 Q16 Q18 Q22 Q24	2N4353
R1 R2	3.9 K
R3	5K TRIMPOT
R4	1 K
R5	1.1 K
C8 C9	1000 PF
Q25 Q27 Q29	2N4351
Q26 Q28	2N4067
Q30	MEM520
R6 R7	10 K
R8	1.5K

FIGURE 66.   TIMING CONTROL
CIRCUIT SCHEMATIC

0467-60A

CLOCK

5.0 MICROSEC

10 MICROSEC

ADDRESS

RESET & DELAY

READ

STROBE DELAY

STROBE

WORD CURRENT

SENSE LINE

DATA REGISTER

(a)   READ AND WRITE MODE

BIT
CURRENT

+35 MA

0 MA

−35 MA
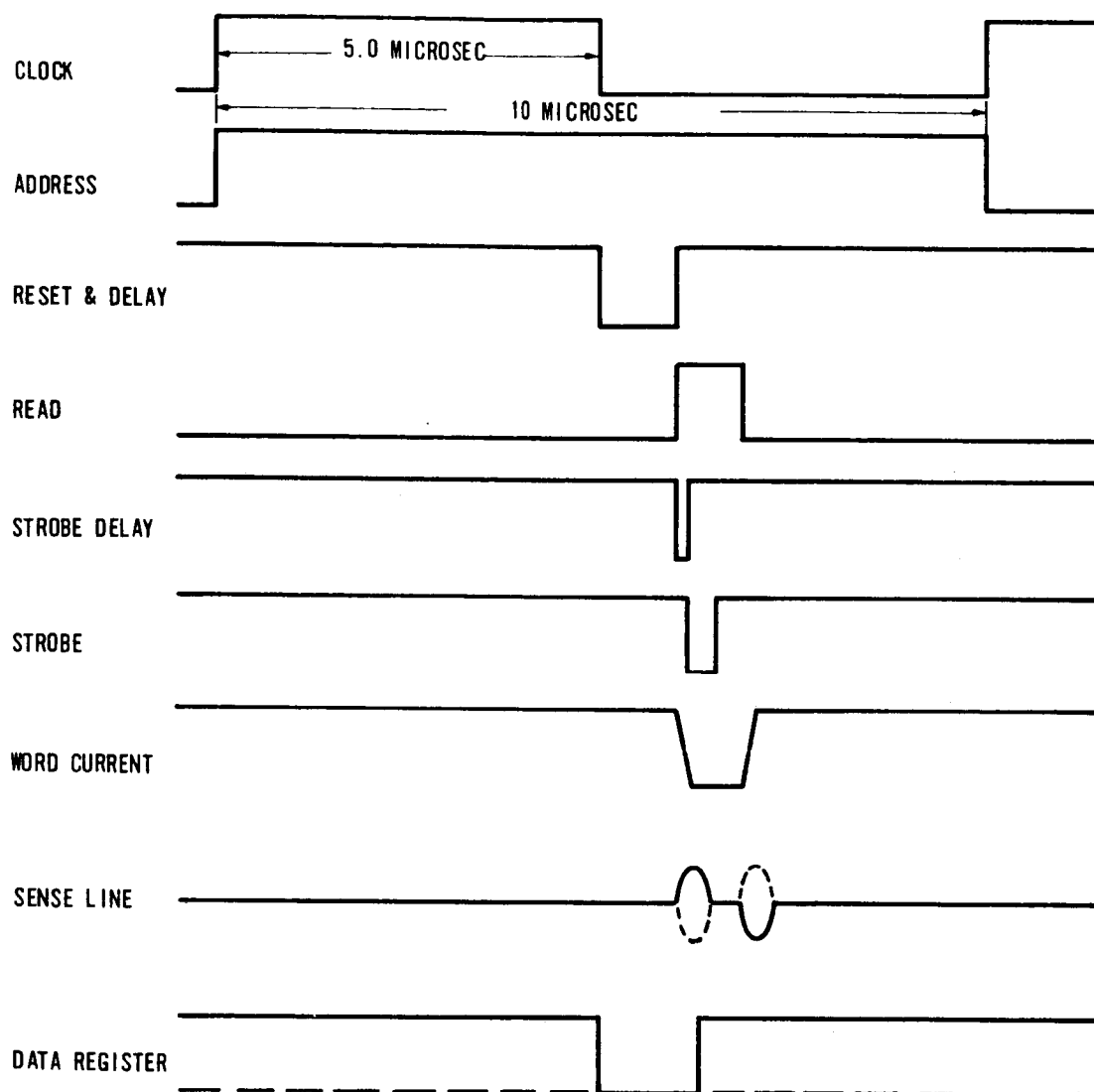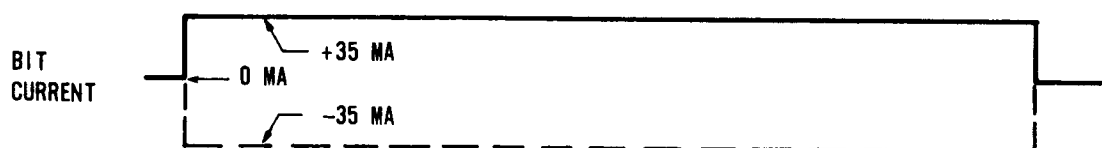
(b)   WRITE MODE ONLY

FIGURE 67.   TIMING DIAGRAM FOR READ AND WRITE
MODES OF OPERATION

0367-23

WORD
CURRENT

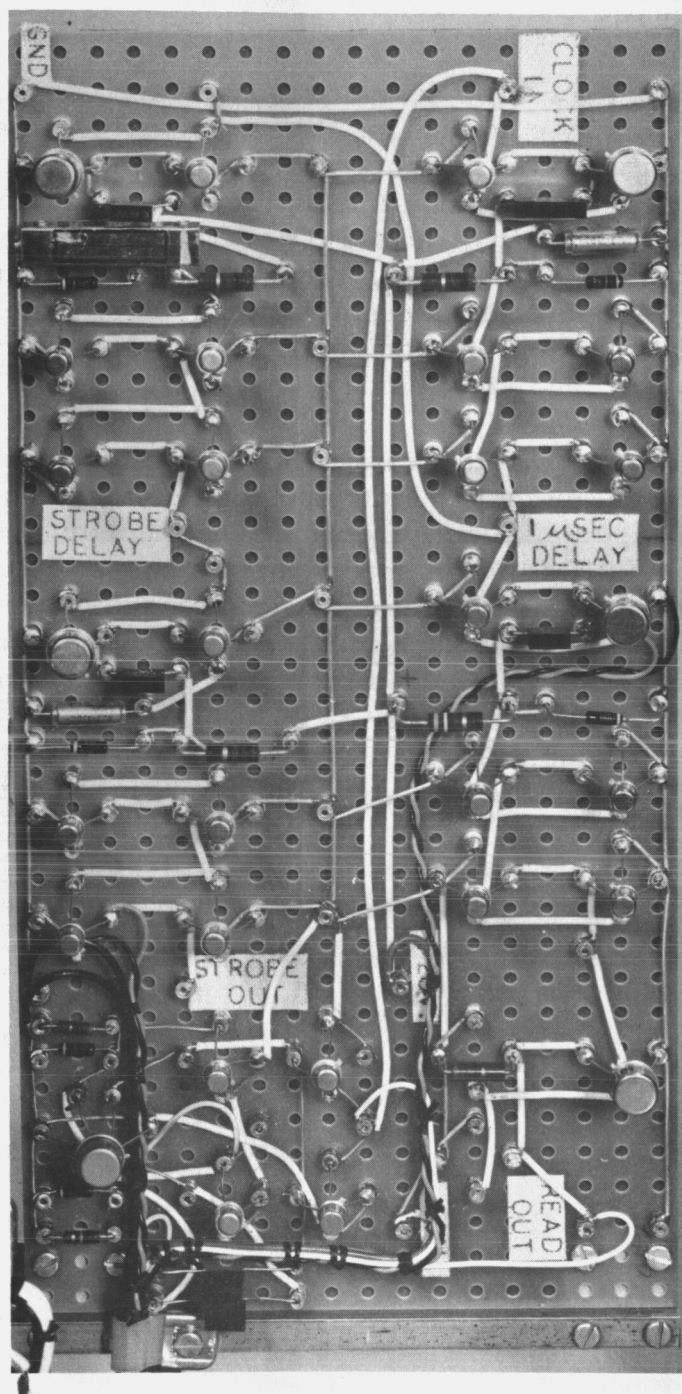100 MA/DIV →

SENSE
AMPLIFIER
OUTPUT →

5.0 VOLTS/DIV

TIME
100 NANOSEC/DIV
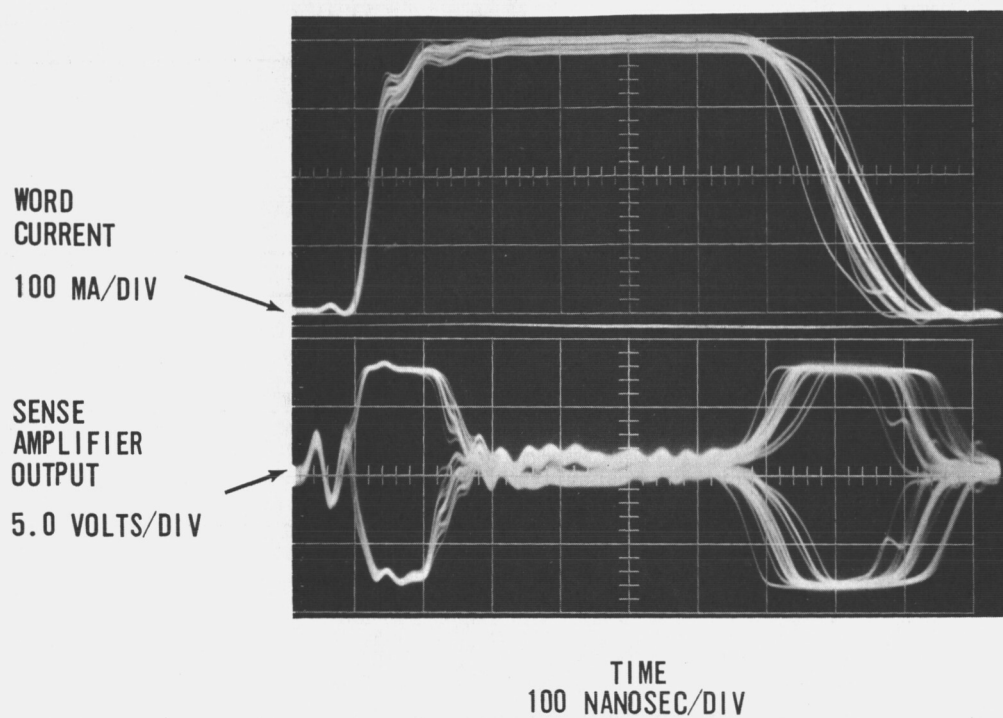
FIGURE 68.   COMPOSITE OF 16-WORD CURRENT AND
SENSE AMPLIFIER OUTPUTS

A6701-60

FIGURE 69.   TIMING AND CONTROL CIRCUIT BOARD

12.0 CONCLUSIONS

Plated wire memories can be designed today which use MOS transistors throughout the memory electronics. These memory systems would operate in the range of 200 kHz. Higher speed memories would normally require the use of bipolar transistors in the timing and control, sense amplifier, and word driver circuits. Operating speeds can be increased above these rates in the future by a reduction in the MOS transistor geometries and/or the operating current requirements of the plated wire. The operating currents of the memory stack can also be reduced by utilizing some advanced plane fabrication techniques.

With the advent of large scale integration (LSI) of MOS transistor circuits, a large portion of the memory electronics can be placed on the same plane as the plated wires, significantly reducing the number of interconnections required. Monometallic interconnect systems presently used by the semiconductor industry to eliminate bimetallic interface problems can be expanded to the system level such that all the interconnections within the memory electronics are performed by a single type of conducting metal.

The speed-power product of MOS transistor circuitry can be considerably improved by a greater utilization of complementary MOS transistor type circuitry. This is presently impeded by the difficulty of fabricating both N and P channel enhancement mode devices in the same chip.

13.0 RECOMMENDATIONS

Future efforts in the advancement of MOS plated wire memory systems should include the following.

1. Reduce MOS transistor geometries in order to obtain lower device capacitances and lower "on" resistance.

2. Develop process for fabricating enhancement mode N channel MOS integrated circuits.

3. Develop plated wire processes or plane fabrication techniques which enable operating currents to be reduced to 100 ma or less while increasing output signal voltage. (This will reduce the requirements on the MOS devices.)

4. Develop manufacturing processes for fabricating high speed, stable MOS differential amplifiers.

5. Develop manufacturing processes for fabricating both N channel and P channel enhancement mode transistors on the same chip.

6. Continued effort in the utilization of a monometallic interconnection system at the daughter board and mother board levels.

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RESEARCH AND DEVELOPMENT Vol. 8, pp 427-429, September 1964.

(7) Heiman, F. P. and Hofstein, S. R., "Metal-Oxide-Semiconductor
Field-Effect Transistors", ELECTRONICS, Vol. 37, pp 50-61,
30 November 1964.

(8) General Microelectronics Inc., Santa Clara, California, MOS
Integrated Circuits Course Notes, 2 May 1966.

(9) Cunningham, J. A., "Expanded Contacts and Interconnections to
Monolithic Silicon Integrated Circuits", SOLID STATE ELECTRONICS,
Vol. 8, pp 735-745, September 1965.

Appendix A

MOS MAGNETIC MEMORY
OPERATING PROCEDURE

CONTROLS DESCRIPTION

1. **POWER**

    Simultaneously turns the -25 volts and +20 volts on and off.

2. **100kHz/SINGLE PULSE**

    Selects either the 100kHz oscillator or the single pulse switch for the basic clock rate.

3. **SINGLE PULSE**

    A pushbutton switch which provides a single clock pulse each time the pushbutton is exercised.

4. **RUN $\frac{\text{START}}{\text{STOP}}$**

    Allows the oscillator to operate at a 100kHz rate when in the RUN position. The START-STOP position is used to start the oscillator when power is first turned on or when the operating mode is changed from SINGLE PULSE to 100kHz. (This switch has no control when the SINGLE PULSE mode of operation is in use.)

5. **FIXED/CYCLING**

    In the fixed position the four toggle switches are used to select any one of 16 addresses. In the CYCLING position the address register operates as a binary counter, cycling sequentially through the 16 addresses.

6. **READ/WRITE**

    Selects either the READ only or the WRITE only mode of operation.

7. **BIT 1 AND BIT 2**

    Selects the polarity of the bit current used in the WRITE mode, hence determining the information stored.

INDICATOR LAMPS

1. <u>ADDRESS LAMPS</u>

   Indicates the address selected.

2. <u>DATA LAMPS</u>

   Displays the information stored in the interrogated address. A "1" is indicated by an "on" lamp. (The display is valid only during the READ mode of operation.)

MODES OF OPERATION

<u>WRITE</u>   <u>READ</u>

MODE 1: 100kHz and cycling   MODE 1: 100kHz and cycling
        address   address
     2: 100kHz and fixed address   2: 100kHz and fixed address
     3: Single pulse and cycling   3: Single pulse and cycling
        address   address
     4: Single pulse and fixed   4: Single pulse and fixed
        address   address

<u>WRITE: MODE 1</u>

This mode of operation is used to write the same information into all 16 words.

<u>CONTROLS</u>	<u>POSITION</u>
CLOCK:	RUN AND 100kHz
BIT WRITE:	"1" OR "0"
READ/WRITE:	WRITE
ADDRESS:	CYCLING

WRITE: MODE 2

This mode of operation is used to write into a fixed address with a large number of word pulses.

CONTROLS	POSITION
CLOCK:	RUN AND 100kHz
BIT WRITE:	"1" OR "0"
READ/WRITE:	WRITE
ADDRESS:	FIXED

WRITE: MODE 3

This mode of operation is used to write one time into the next higher address than the address presently being displayed by the indicator lamps.

CONTROLS	POSITION
CLOCK:	SINGLE PULSE
BIT WRITE:	"1" OR "0"
READ/WRITE:	WRITE
ADDRESS:	CYCLING

WRITE: MODE 4

This mode of operation is used to write one or more times into a fixed address as selected by the address switch.

CONTROLS	POSITION
CLOCK:	SINGLE PULSE
BIT WRITE:	"1" OR "0"
READ/WRITE:	WRITE
ADDRESS:	FIXED

READ: MODE 1

This mode of operation disturbs all 16 words with word pulses by continuously cycling through the memory at a 100kHz rate.

CONTROLS	POSITION
CLOCK:	RUN AND 100kHz
BIT WRITE:	NOT USED
READ/WRITE:	READ
ADDRESS:	CYCLING

READ: MODE 2

This mode of operation is used to continuously read a fixed address as selected by the address switches.

CONTROLS	POSITION
CLOCK:	RUN AND 100kHz
BIT WRITE:	NOT USED
READ/WRITE:	READ
ADDRESS:	FIXED

READ: MODE 3

This mode of operation is used to read out the information stored in the next higher address than the address presently being displayed by the indicator lamps.

CONTROLS	POSITION
CLOCK:	SINGLE PULSE
BIT WRITE:	NOT USED
READ/WRITE:	READ
ADDRESS:	CYCLING

READ: MODE 4

This mode of operation is used to read one or more times from a fixed
address as selected by the address switches.

CONTROLS	POSITION
CLOCK:	SINGLE PULSE
BIT WRITE:	NOT USED
READ/WRITE:	READ
ADDRESS:	FIXED

Appendix B

MANUFACTURER'S SPECIFICATION
SHEETS FOR MOS DEVICES

General Instruments MEM 517
General Instruments MEM 517A
General Instruments MEM 520
General Instruments MEM 1002
General Instruments MEM 1005
General Instruments 2N 4353
Motorola   2N 4351
Fairchild   F 10049
Fairchild   2N 4067
RCA   3N 128

0467-81N

POWER MOS TRANSISTOR

Technical Specifications
August, 1966

P CHANNEL–ENHANCEMENT MODE
SILICON INSULATED GATE
FIELD EFFECT TRANSISTOR

MEM 517

GENERAL INSTRUMENT

FEATURES:

- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS:

($T_A = 25°C$, unless otherwise specified)

Drain to Source Voltage	—30V
Gate to Source Voltage	—25V
Gate to Drain Voltage	—25V
Drain Current	—250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	—50 to 150°C
Operating Junction Temperature	—50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watt

ELECTRICAL CHARACTERISTICS:

($T_A = 25°C$, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	—2.5		—5	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		—0.8	—50	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current		—0.1	—1	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	—25	—60		mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	—30	—50		Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
BV_{GSS}	Gate to Source Breakdown	—25	—40		Volts	$I_{GS} = -10\mu A$, $V_{DS} = 0V$
Y_{fs}	Transadmittance		12000		μmho	1 kHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance		10		pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance		10		pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		0.15		pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	$V_{GS} = -20V$, $I_{DS} = -10mA$
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	$V_{GS} = -10V$, $I_{DS} = -10mA$

TO-33

.370 / .335 DIA.

.335 / .305 DIA.

.100 MIN.

.260 / .240

.009 / .125

.050

SEATING PLANE

.012 / .016 DIA.

1.5 MIN.

.016 / .021 DIA.

.200

.250

.100

.007r MAX.

45°

.200

.034 / .028

.100

.045 / .029

Bottom view

Note: All dimensions in inches.

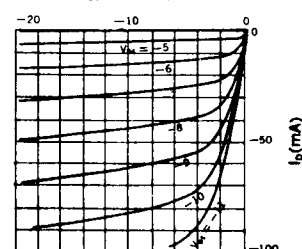### TERMINAL DIAGRAM
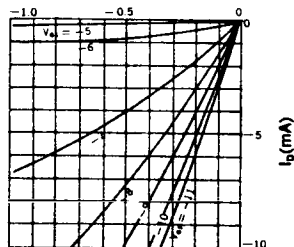
Lead
1. Drain
2. Gate
3. Body (Case)
4. Source
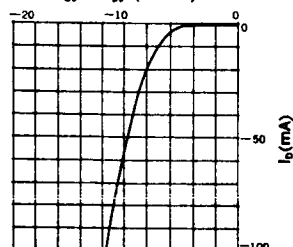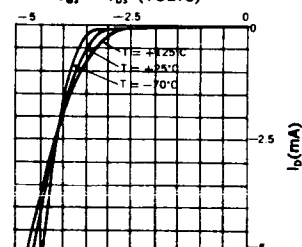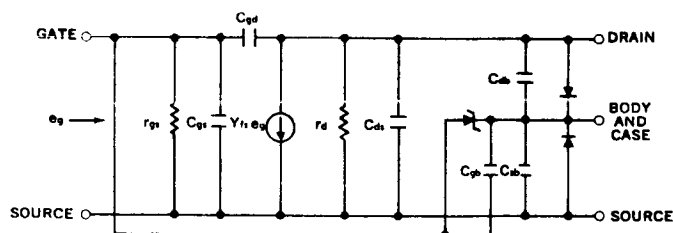
P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

MEM 517

0467-82N

TYPICAL CHARACTERISTIC CURVES
MEM 517

DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)

DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)

DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)

DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)

TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)

SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$

HANDLING PRECAUTIONS

MEM 517 insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10¹⁵ ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10¹⁵	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	10	pF
C_{gd}	Gate to drain capacitance	10	pF
C_{ds}	Drain to source capacitance	0.15	pF
C_{gb}	Gate to body capacitance	6	pF
C_{db}	Drain to body capacitance	10	pF
C_{sb}	Source to body capacitance	20	pF
Y_{fs}	Forward transadmittance	12000	μmho

SEMICONDUCTOR PRODUCTS GROUP

MICROELECTRONIC DIVISION

B-3

0467-83N

POWER MOS TRANSISTOR

GENERAL INSTRUMENT

P CHANNEL-ENHANCEMENT MODE
SILICON INSULATED GATE
FIELD EFFECT TRANSISTOR

Technical Specifications
November, 1965

MEM 517A

P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR

MEM 517A

FEATURES:
- 10^{10} ohms input resistance
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS:
(Designed Primarily For Low-Power Audio, Radio Frequency and Commutating Applications.)
- Audio output stages
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF power amplifiers
- Multiplexers

MAXIMUM RATINGS:
($T_A = 25°C$, unless otherwise specified)

Drain to Source Voltage	—30V
Gate to Source Voltage	—25V
Gate to Drain Voltage	—25V
Drain Current	—250mA
Gate Current (Forward Direction for Zener Clamp)	+1.0mA
Storage Temperature	—50 to 150°C
Operating Junction Temperature	—50 to 125°C
Total Dissipation at 25°C Case Temperature	2.0 Watts
Total Dissipation at 25°C Ambient Temperature	0.6 Watts

ELECTRICAL CHARACTERISTICS:
($T_A = 25°C$, unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	—2.5		—5	Volts	$V_{GS} = V_{DS}$, $I_D = —10\mu A$
I_{DSS}	Drain Leakage Current		0.8	—50	nA	$V_{DS} = —20V$, $V_{GS} = 0$
I_{GSS}	Gate Leakage Current		0.1	—1	nA	$V_{GS} = —15V$, $V_{DS} = 0$
$I_{D(on)}$	Drain Current		—60		mA	$V_{GS} = V_{DS} = —10V$
BV_{DSS}	Drain-Source Breakdown	—30	—50		Volts	$I_D = —10\mu A$, $V_{GS} = 0$
BV_{GSS}	Gate to Source Breakdown	—25	—40		Volts	$I_{GS} = —10\mu A$, $V_{DS} = 0$
Y_{fs}	Transadmittance		12000		μmho	1KC, $V_{GS} = V_{DS} = —10V$
C_{gs}	Gate to Source Capacitance		16		pf	$V_{GS} = V_{DS} = —10V$
C_{gd}	Gate to Drain Capacitance		10		pf	$V_{GS} = V_{DS} = —10V$
C_{ds}	Drain to Source Capacitance		10		pf	$V_{GS} = V_{DS} = —10V$
$r_{DS(on)}$	Drain to Source on Resistance		25		Ohms	$V_{GS} = —20V$, $I_{DS} = —10mA$
$r_{DS(on)}$	Drain to Source on Resistance		45		Ohms	$V_{GS} = —10V$, $I_{DS} = —10mA$

TO-5 PACKAGE

.370 / .335 DIA.
.335 / .305 DIA.
.100 MIN.
.260 / .240
.009 / .125
1.5 MIN.
.019 / .016 DIA.
.200
.100
MAX. OUTSIDE CORNER RADII .007
.100
.200
45°
.034 / .028
.045 / .029
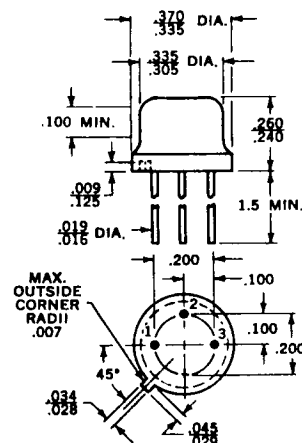
Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Source & Body (Case)
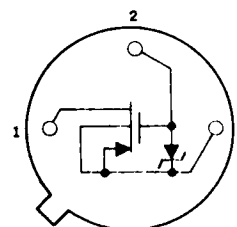
TYPICAL CHARACTERISTIC CURVES
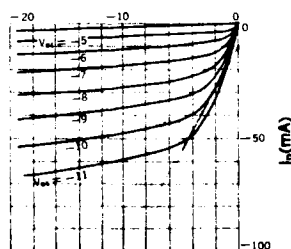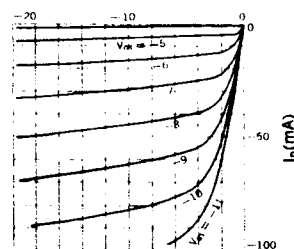### MEM 517A
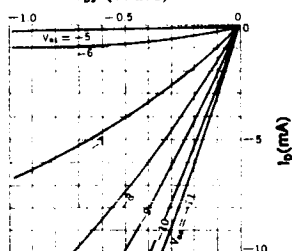
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)
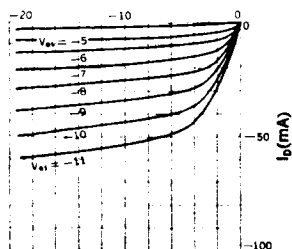
DRAIN CHARACTERISTICS AT 25°C
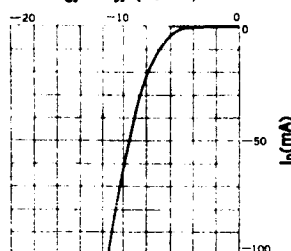V_{DS} (VOLTS)

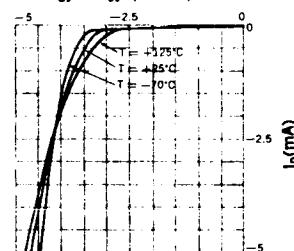**DRAIN CHARACTERISTICS AT −70°C**
V_{DS} (VOLTS)

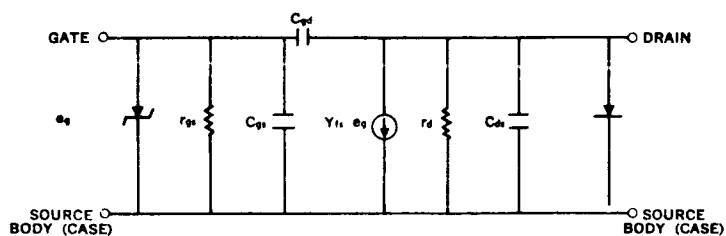**DRAIN CHARACTERISTICS AT 25°C**
V_{DS} (VOLTS)

TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)

SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 60mA$

SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{gs}	Gate to source leakage resistance and diode leakage resistance	10^{10}	ohms
r_d	Dynamic drain resistance	1.0	Kohms
C_{gs}	Gate to source capacitance	16	pf
C_{gd}	Gate to drain capacitance	10	pf
C_{ds}	Drain to source capacitance	10	pf
Y_{fs}	Forward transadmittance	12000	μmho

HANDLING PRECAUTIONS

MEM 517A insulated gate field effect transistors have been designed with an integrated zener diode which clamps the high internal resistance (10^{15} ohm typical) gate, to the body. This clamp eliminates the detrimental effects of high electrostatic voltages on the gate that can be generated in normal handling.

SEMICONDUCTOR PRODUCTS GROUP

0467-66N

GENERAL INSTRUMENT

MOS TRANSISTOR

P CHANNEL–ENHANCEMENT MODE
SILICON INSULATED GATE
FIELD EFFECT TRANSISTOR

Technical Specifications
August, 1966

MEM 520

FEATURES:

- 10^{15} ohms Input resistance
- Normally off with zero gate voltage
- Square Law linear transfer characteristics

APPLICATIONS:

(Designed Primarily For Power Audio, Radio Frequency and Commutating Applications.)

- Very high input impedance amplifiers
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- RF and IF amplifiers
- Multiplexers

MAXIMUM RATINGS:

(T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	—30V
Gate to Source Voltage	—40V
Gate to Drain Voltage	—40V
Drain Current	—50mA
Storage Temperature	—50 to 150°C
Operating Junction Temperature	—50 to 125°C
Total Dissipation at 25°C Case Temperature	650mW
Total Dissipation at 25°C Ambient Temperature	225mW

ELECTRICAL CHARACTERISTICS:

(T_A = 25°C, unless otherwise specified — body grounded).

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{GST}	Gate Source Cutoff Voltage	—3		—6	Volts	$V_{GS} = V_{DS}$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current		—0.5	—10	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{GSS}	Gate Leakage Current		—.03	—3	nA	$V_{GS} = -40V$, $V_{DS} = 0V$
$I_{D(on)}$	Drain Current	—3			mA	$V_{GS} = V_{DS} = -10V$
BV_{DSS}	Drain-Source Breakdown	—30			Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
Y_{fs}	Transadmittance	1000 1000			μmho μmho	1 kHz, $V_{GS} = V_{DS} = -10V$ 10 MHz, $V_{GS} = V_{DS} = -10V$
C_{gs}	Gate to Source Capacitance			3	pF	$V_{GS} = V_{DS} = -10V$
C_{gd}	Gate to Drain Capacitance			2.5	pF	$V_{GS} = V_{DS} = -10V$
C_{ds}	Drain to Source Capacitance		.15		pF	$V_{GS} = V_{DS} = -10V$
$r_{DS(on)}$	Drain to Source Resistance		150		ohms	$V_{GS} = -15V$, $I_{DS} = -1mA$

TO-72 PACKAGE
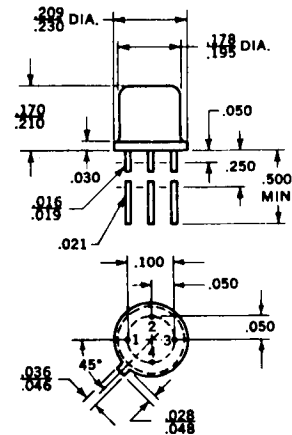
.209/.230 DIA.
.178/.195 DIA.
.170/.210
.050
.030
.250
.500 MIN.
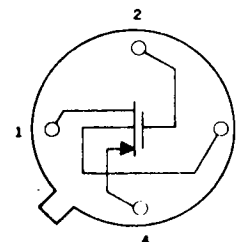.016/.019
.021
.100
.050
.050
45°
.036/.046
.028/.048

Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Body (Case)
4. Source

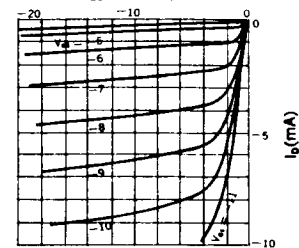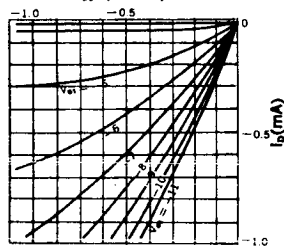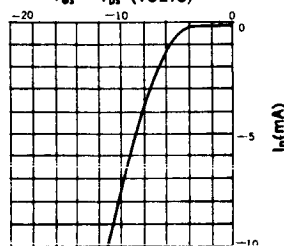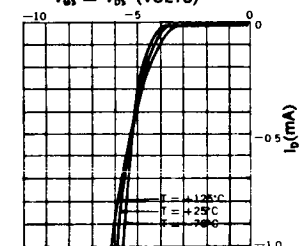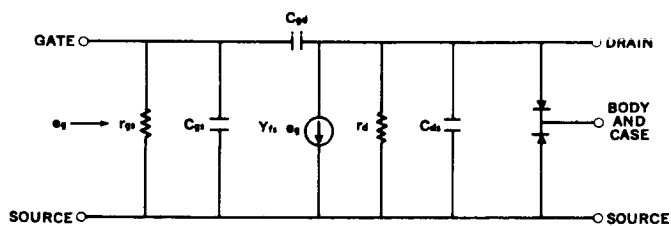P CHANNEL–ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR MEM 520

SEMICONDUCTOR PRODUCTS GROUP

TYPICAL CHARACTERISTIC CURVES
MEM 520

0467-86N

DRAIN CHARACTERISTICS AT 125°C
V_DS (VOLTS)

DRAIN CHARACTERISTICS AT 25°C
V_DS (VOLTS)

DRAIN CHARACTERISTICS AT −70°C
V_DS (VOLTS)

DRAIN CHARACTERISTICS AT 25°C
V_DS (VOLTS)

TURN-ON CHARACTERISTICS AT 25°C
V_GS = V_DS (VOLTS)

TURN-ON CHARACTERISTICS
V_GS = V_DS (VOLTS)

SMALL SIGNAL EQUIVALENT CIRCUIT
(Conditions: $V_{GS} = V_{DS} = -10V$)
$I_D \approx 6mA$

GATE — C_gd — DRAIN

e_g — r_gs — C_gs — Y_fs e_g — r_d — C_ds — BODY AND CASE

SOURCE — SOURCE

HANDLING PRECAUTIONS

The MEM 520 insulated gate field effect transistors have very high gate resistance, (10^{15} ohm typical). This resistance, combined with the gate capacitance, requires that every precaution be taken during testing and handling in order to prevent charge build up and possible gate breakdown.

The shorting of the gate lead to the other leads during handling will protect the gate from breakdown.

SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_gs	Gate to source leakage resistance	10^{15}	ohms
r_d	Dynamic drain resistance	10	Kohms
C_gs	Gate to source capacitance	2.25	pF
C_gd	Gate to drain capacitance	1.5	pF
C_ds	Drain to source capacitance	0.15	pF
Y_fs	Forward transadmittance	2500	μmho

SEMICONDUCTOR PRODUCTS GROUP

MICROSEMICONDUCTOR DIVISION
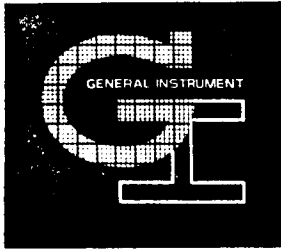
GENERAL INSTRUMENT
MOS INTEGRATED CIRCUIT

ADVANCE
May, 1966

DUAL 3-INPUT NOR-GATE

MEM 1002

DESCRIPTION

The MEM 1002 is a dual three input NOR gate constructed on a single mono-lithic chip utilizing MOS P-channel enhancement mode transistors. It is a rugged, low power consumption unit designed for use in timing, decoding and multiplexing applications.

OPERATION

The MEM 1002 is described by the following logic equation:

$$\text{Each Output} = \overline{A + B + C}$$

FEATURES

- Buffered outputs
- High input impedance
- High noise immunity
- Large fanout
- Low power consumption
- Monolithic construction

MAXIMUM RATINGS

Drain Voltage (V_{DD})	−30 V to +.3 V
Logic Input Voltage	−30 V to +.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

ELECTRICAL CHARACTERISTICS

$V_{DD} = 27$ Volts ±1 Volt, $R_L = 10M\Omega$, $C_L = 10pF$. $T_A = -55°C$ to $+85°C$ (unless otherwise specified)

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
Logic "0"	—	—	−2.0	Volts	dc
Logic "1"	−10	—	—	Volts	dc
Frequency	dc	—	500	kHz	
Pulse Width	500	—	—	ns	
Fan-In	—	—	1.0		
Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Outputs					
Logic "0"	—	−0.5	−1.0	Volt	dc
Logic "1"	−11	−12	—	Volts	
Propagation Delay Plus Rise Time $t_{(pd1)}$	—	300	400	ns	SEE FIG. 1
Propagation Delay Plus Fall Time $t_{(pd2)}$	—	400	600	ns	SEE FIG. 1
Fan-Out	—	—	5.0		
Impedance to Ground	—	3000	5500	Ohms	$V_{in} = -10$ Volts
Drive Capability	−10	−11	—	Volts	$V_{in} = 0$ Volts $R_L = 17K$ Ohms
Drive Capability	−5.0	—	—	Volts	$V_{in} = 0$ Volts $R_L = 4K$ Ohms
Capacitance	—	3.0	5.0	pF	$V_O = 0$ Volts
Supply Current Drain per Gate	—	—	0.55	mA	

LOW PROFILE 10 LEAD TO—74
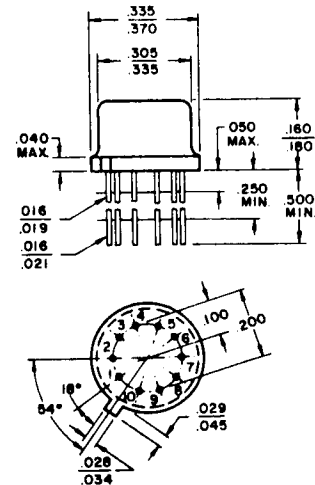
Note: All dimensions in inches

TERMINALS

P/N	Function
1	Input A1
2	Input B1
3	Input C1
4	Output 1
5	Ground
6	Input A2
7	Input B2
8	Input C2
9	Output 2
10	−V_{DD}

GENERAL INSTRUMENT CORPORATION

FIGURE 1
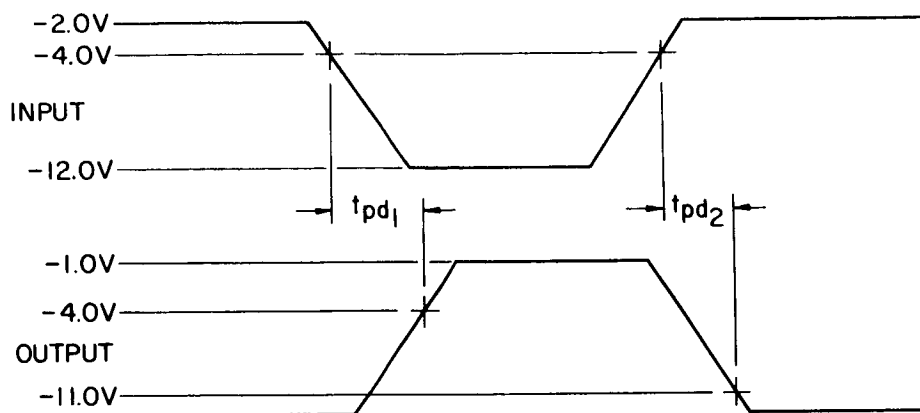
LOGIC DIAGRAM
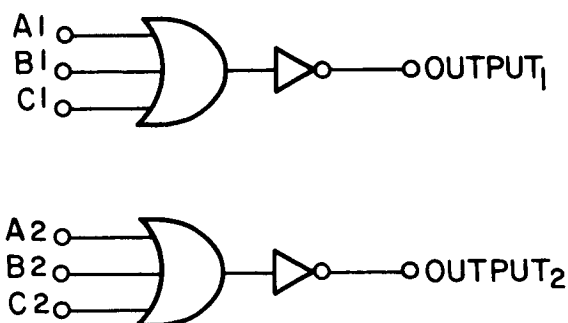
GENERAL INSTRUMENT CORPORATION

MICROELECTRONIC DIVISION

GENERAL INSTRUMENT
MOS INTEGRATED CIRCUIT

ADVANCE
May, 1966

R-S-T FLIP-FLOP

MEM 1005

DESCRIPTION

The MEM 1005 R-S-T Flip-Flop is constructed on a single monolithic chip utilizing MOS P-channel enhancement mode transistors. The flip-flop outputs trigger on the negative going edge of the clock. The set and reset inputs are complementary inputs. The unit also has direct set and reset inputs.

MAXIMUM RATINGS

Clock and Input Voltage	$-30V$ to $+.3V$
Drain Voltage $(-V_{dd})$	$-30V$ to $+.3V$
Storage Temperature	$-55°C$ to $+150°C$
Operating Temperature	$-55°C$ to $+85°C$

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified):
$V_{dd} = -27$ Volts ± 1 Volt, Load $= 10M\Omega$ and 10pF.
$T_A = -55°C$ to $+85°C$.

LOGIC DIAGRAM

Direct Set

$\overline{S} \rightarrow$ ... $\rightarrow Q$
$T \rightarrow$
$R \rightarrow$ ... $\rightarrow \overline{Q}$

Direct Reset
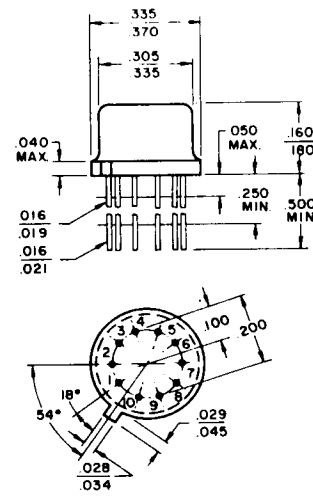
CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Inputs & Clock					
Logic "0"	0	—	−2.0	Volts	
Logic "1"	−10	—	—	Volts	
Frequency	dc	—	500	kHz	
Pulse Width (ϕ_{pw})	400	—	—	nsec.	SEE FIG. 1
Clock Pulse Rise and Fall Time (10% to 90%)	—	—	20.0	μsec.	
Leakage Current	—	—	1.0	μA	$V_{in} = -20$ Volts
Clock Fan-In	—	—	3.0		
Set, Reset, Direct Set & Reset Fan-In	—	—	1.0		dc to 500 kHz
Outputs					
Logic "0"	—	−0.5	−1.0	Volt	dc to 500 kHz
Logic "1"	−11	−12	—	Volts	dc to 500 kHz
Propagation Delay and Fall Time (t_{pd1})	—	—	950	nsec.	SEE FIG. 1
Propagation Delay and Rise Time (t_{pd2})	—	—	500	nsec.	SEE FIG. 1
Fan-Out	—	—	5		
Noise Immunity	1.0	—	—	Volt	dc to 500 kHz
Capacitance	—	2.0	4.0	pF	$V_O = 0$ Volts
Impedance to Ground (Output a Logic "0")	—	—	2000	Ohms	
Drive Capability	−10	−11	—	Volts	$R_L = 17K$ Ohms
Drive Capability	−5.0	—	—	Volts	$R_L = 4K$ Ohms
Supply Current	—	—	2.6	mA	

LOW PROFILE 10 LEAD
TO–74

.335 / .370
.305 / .335
.040 MAX.
.050 MAX.
.160 / .180
.016 / .019
.016 / .021
.250 MIN.
.500 MIN.

.100 .200
18° 54°
.029 / .045
.028 / .034

Note: All dimensions in inches.

TERMINALS

P/N	Function
1	Direct Reset Input
2	True Output (Q)
3	Reset Input
4	Clock Input
5	Ground
6	Set Input
7	False Output $(\overline{Q})$
8	Direct Set Input
9	No Connection
10	Drain Voltage $(-V_{dd})$

0467-90N
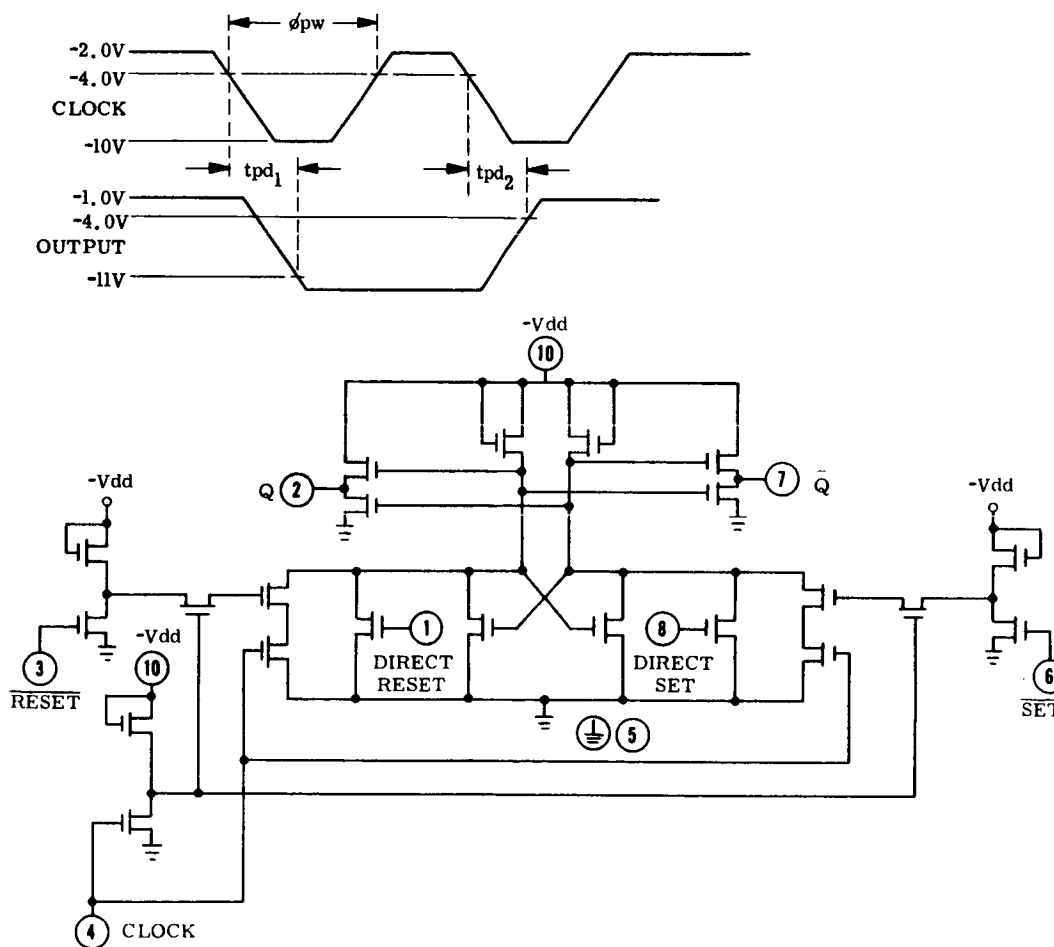
TYPICAL TIMING DIAGRAM (Binary Mode of Operation)
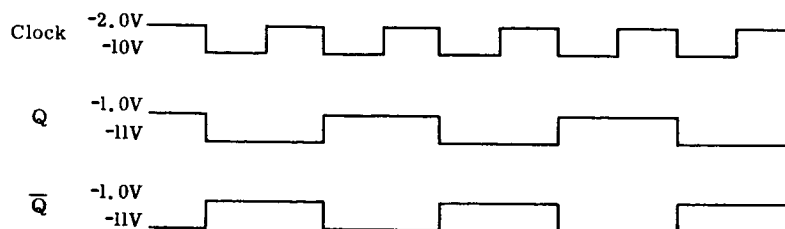
NOTE: Direct set and reset must be tied to a Logical "0".

FIGURE 1

GENERAL INSTRUMENT CORPORATION

MICROELECTRONIC DIVISION

Printed in U.S.A.

T-6020

B-11

0467-91N

GENERAL INSTRUMENT

MOS TRANSISTOR

P CHANNEL-ENHANCEMENT MODE
SILICON INSULATED GATE
FIELD EFFECT TRANSISTOR

TECHNICAL SPECIFICATIONS
AUGUST, 1966

2N4353

FEATURES
• 10^{12} ohms input resistance • Normally off with zero gate voltage • Square Law transfer characteristics

APPLICATIONS
• Very high input impedance amplifiers
• Series and shunt choppers
• Operational amplifiers
• Logic circuits
• Linear RF and IF amplifiers
• Multiplexers
• Analog switches

MAXIMUM RATINGS:

Temperature
Storage Temperature Range, T_{stg} .... −60°C to 125°C
Lead (Terminal) Temperature, ⅟₁₆″ from
the seated surface (or case) for 10 seconds .... 230°C

Voltage at 25°C Free-Air Temperature
Forward Gate-Source Voltage .... −30V
Drain-Source Voltage .... −25V
Drain-Gate Voltage .... −25V

Current
Reverse Gate Current .... +1 mA
Forward Gate Current .... −.01 mA
Drain Current .... −100 mA

Power
Continuous Device Dissipation at or below 25°C Free-Air Temperature .... 250 mW
Linear Derating Factor .... 2 mW/°C

TO-72

.230/.209 DIA.
.195/.178 DIA.
.210/.170
.030
.050 MAX.
.250 MIN. .500 MIN.
SEATING PLANE
.019/.016 DIA.
.021/.016 DIA.
.100
.050
.050
.100
45°
.048/.036
.048/.028

Bottom view
NOTE: All dimensions in inches

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$I_{G(f)}$	Gate Forward Current		−1.0	nA	$V_{GS} = -20V, V_{DS} = 0V$
$I_{G(f)}$	Gate Forward Current		−100	nA	$V_{GS} = -20V, V_{DS} = 0V, T_A = 85°C$
$V_{(BR)GSS}$	Gate-Source Reverse Breakdown Voltage		+3.0	V	$I_G = 1$ mA, $V_{DS} = 0V$
$V_{GS(f)}$	Gate-Source Forward Voltage	−30	−60	V	$I_G = -.01$ mA, $V_{DS} = 0V$
$I_{D(on)}$	"ON" Drain Current	−30		mA	$V_{DS} = -10V, V_{GS} = -20V$ Pulse Test: 300 μs pw, 2% Duty Cycle
V_{GS}	Gate-Source Voltage	−5.0	−10	V	$V_{DS} = -10V, I_D = -10$ mA
$V_{GS(th)}$	Gate-Source Threshold Voltage	−2.5	−5.0	V	$V_{DS} = -10V, I_D = -10$ μA
I_{DSS}	Zero-Gate-Voltage Drain Current		−5	nA	$V_{DS} = -10V, V_{GS} = 0$
$r_{DS(on)}$	Static Drain-Source "ON" Resistance		300	Ohms	$I_D = -0.1$ mA, $V_{GS} = -20V$
Y_{fs}	Transadmittance	1000	4000	Ohms	$V_{DS} = -10V, I_D = -10$ mA
Y_{os}	Output Admittance		350	μmhos	1 kHz $V_{DS} = -10V, I_D = -10$ mA
C_{iss}	Input Capacitance		12	oF	1 MHz $V_{DS} = -10V, I_D = -10$ mA
C_{rss}	Reverse Transfer Capacitance		4	pF	1 MHz $V_{DS} = -10V, I_D = -10$ mA
C_{DGO}	Drain-Gate Capacitance		4	pF	1 MHz $V_{DG} = -10V, I_S = 0$
$R_{e(Yfs)}$	Forward Transconductance	900		μmhos	30 MHz $V_{DS} = -10V, I_D = -10$ mA
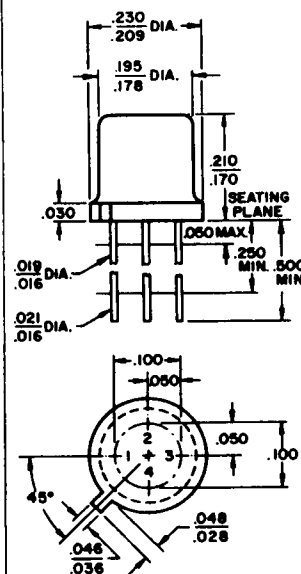
TERMINALS

P/N	FUNCTION
1	Drain
2	Gate
3	Body (Case)
4	Source

NOTE: Case Material — Metallic
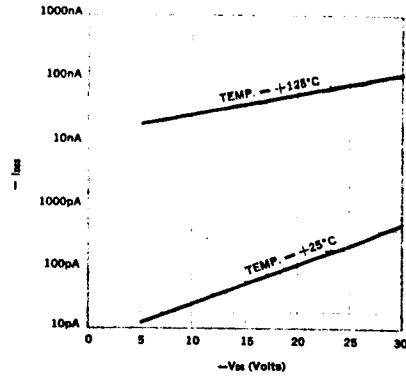(Electrically Non-Insulated)

TERMINAL DIAGRAM

MICROELECTRONIC DIVISION
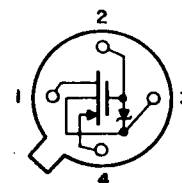
P CHANNEL-ENHANCEMENT MODE SILICON INSULATED GATE FIELD EFFECT TRANSISTOR   2N4353
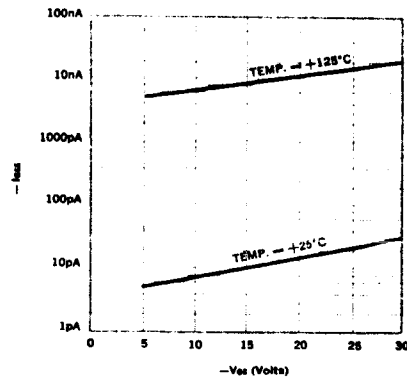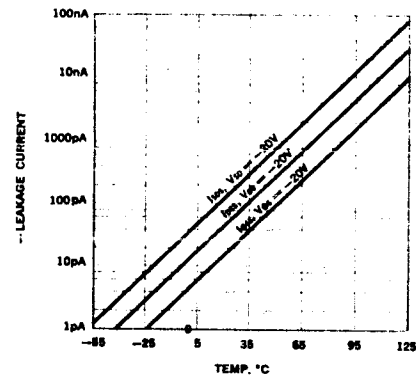
0487-92N

DRAIN LEAKAGE VS DRAIN VOLTAGE

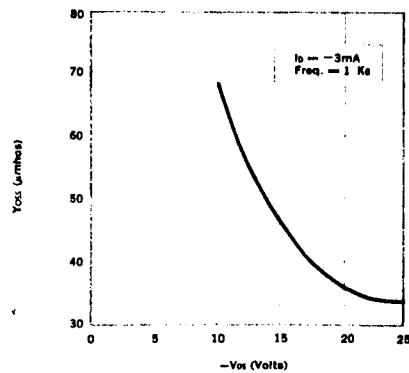**SOURCE LEAKAGE VS SOURCE VOLTAGE**
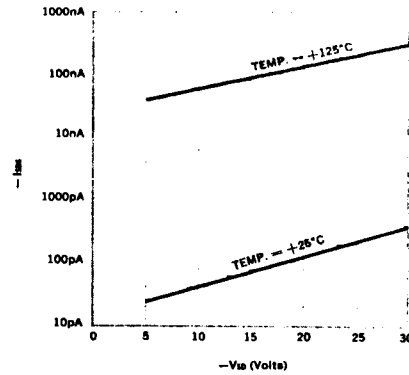
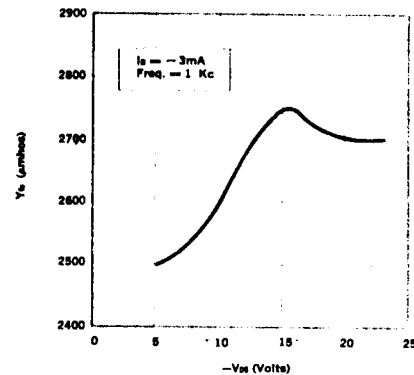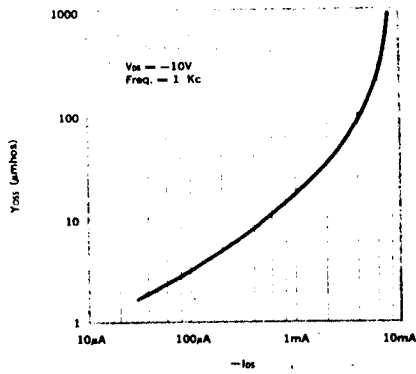**GATE LEAKAGE VS GATE VOLTAGE**

LEAKAGE CURRENT VS TEMPERATURE
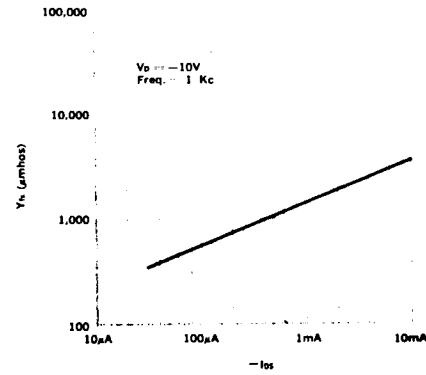
OUTPUT ADMITTANCE VS DRAIN VOLTAGE
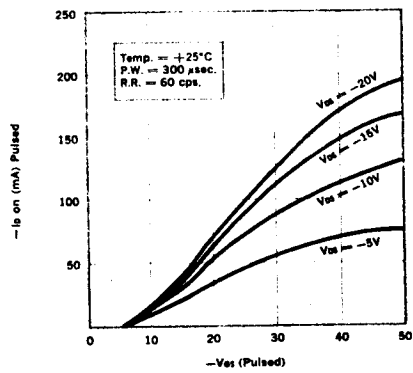
FORWARD TRANSADMITTANCE VS DRAIN VOLTAGE

0467-93N

OUTPUT ADMITTANCE VS DRAIN CURRENT

$V_{DS} = -10V$
Freq. = 1 Kc

Y_{OSS} (µmhos)

$-I_{DS}$

FORWARD TRANSADMITTANCE VS DRAIN CURRENT

$V_D = -10V$
Freq. = 1 Kc

Y_{fs} (µmhos)

$-I_{DS}$

DRAIN CURRENT (PULSED) VS GATE VOLTAGE (PULSED)

Temp. = +25°C
P.W. = 300 µsec.
R.R. = 60 cps.

$V_{GS} = -20V$
$V_{GS} = -15V$
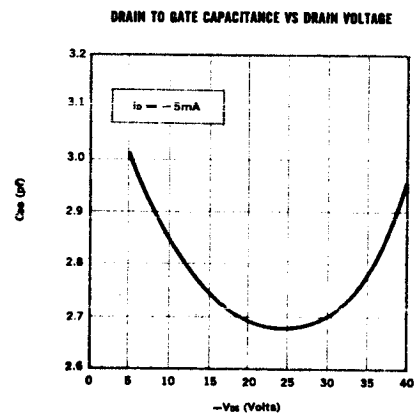$V_{GS} = -10V$
$V_{GS} = -5V$

$-I_D$ on (mA) Pulsed

$-V_{DS}$ (Pulsed)

GATE VOLTAGE VS BODY TO SOURCE VOLTAGE

$V_{DS} = -0.5V$
$I_D = -1µA$
Temp. = 25°C

$-V_{GS}$ (Volts)

$+V_{BS}$ (Volts)

GATE VOLTAGE VS BODY TO SOURCE VOLTAGE

$I_D = -10µA$
$V_{DS} = -10V$
Temp. = +25°C

$-V_{GS}$ (Volts)

$+V_{BS}$ (Volts)

DRAIN CURRENT VS GATE VOLTAGE

$V_{DS} = -20V$

-55°C   25°C
125°C

125°C   25°C   -55°C

$-V_{GS}$ (Volts)

0467-94N

INPUT CAPACITANCE VS DRAIN CURRENT

INPUT CAPACITANCE VS DRAIN VOLTAGE

DRAIN TO GATE CAPACITANCE VS DRAIN CURRENT

DRAIN TO GATE CAPACITANCE VS DRAIN VOLTAGE

OUTPUT CAPACITANCE VS DRAIN VOLTAGE
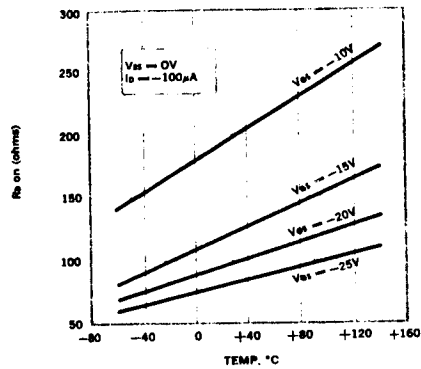
OUTPUT CAPACITANCE VS DRAIN CURRENT
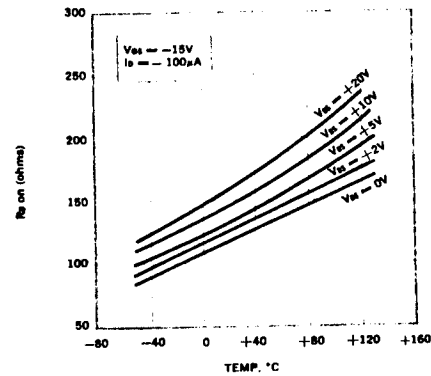
GI [ELECTRICAL CHARACTERISTICS]

DYNAMIC DRAIN RESISTANCE VS TEMPERATURE

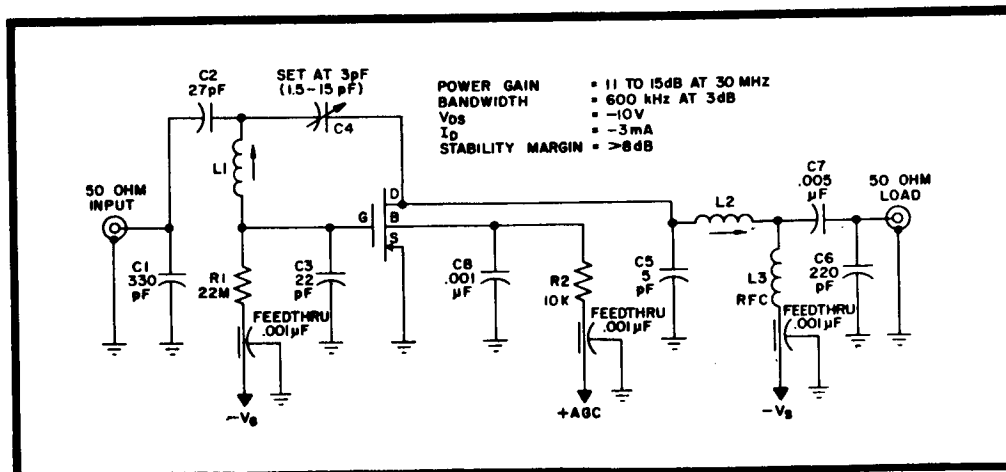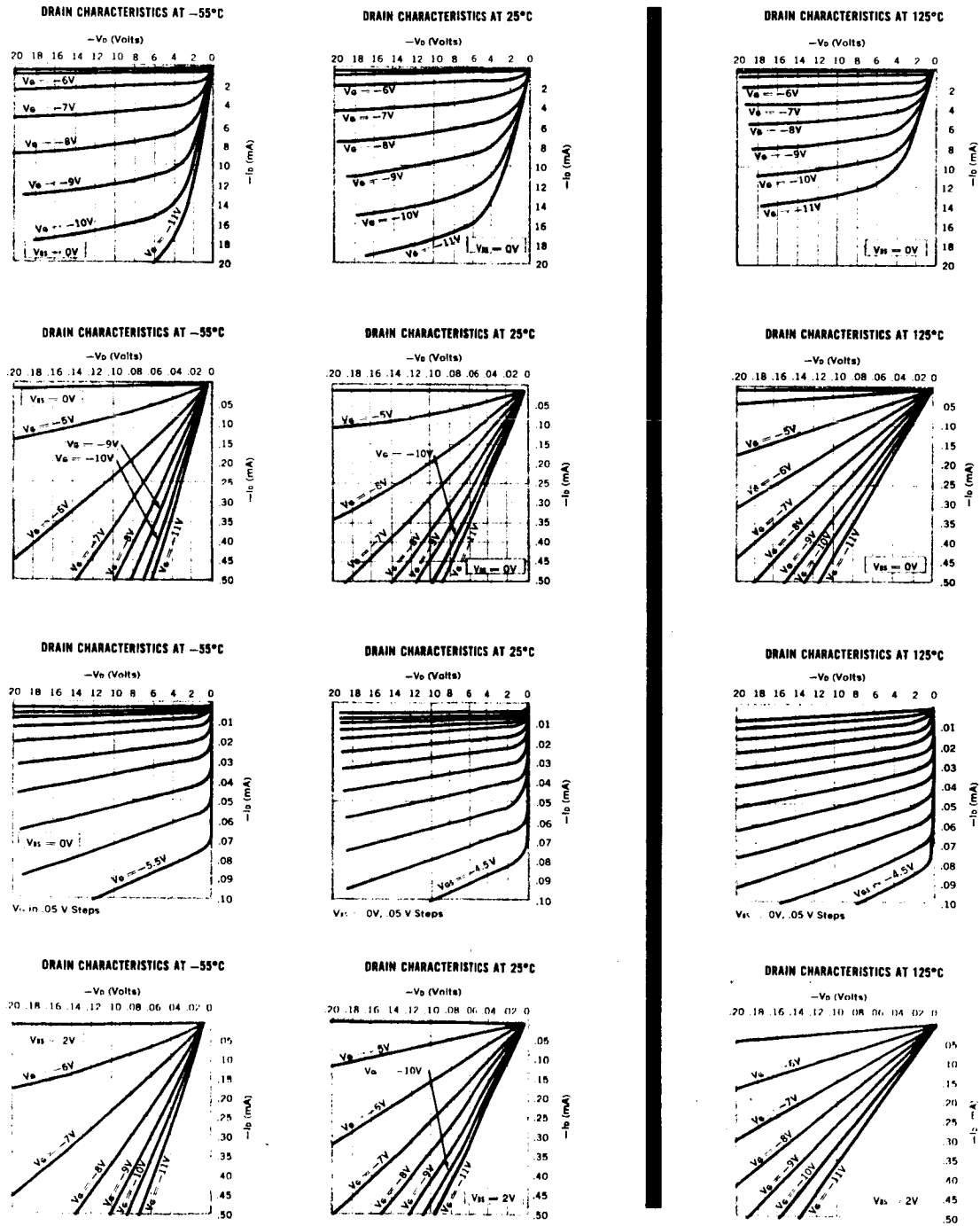**DYNAMIC DRAIN RESISTANCE VS TEMPERATURE**

APPLICATIONS
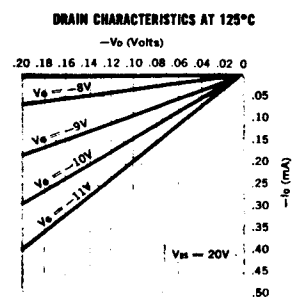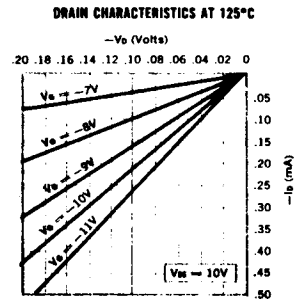
30 MHz Amplifier Utilizing a 2N4353
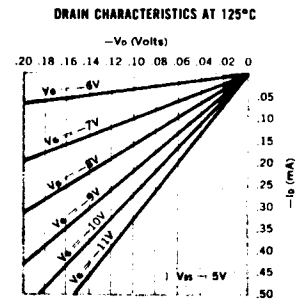
0487-96N

TYPICAL CHARACTERISTIC CURVES

All curves have been plotted from photographs taken with a Tektronix Curve Tracer, Model 575

DRAIN CHARACTERISTICS AT −55°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −9V

V₉ = −10V

Vᵦₛ = 0V

−Iᴅ (mA): 2, 4, 6, 8, 10, 12, 14, 16, 18, 20

DRAIN CHARACTERISTICS AT 25°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −9V

V₉ = −10V

V₉ = −11V   Vᵦₛ = 0V

−Iᴅ (mA): 2, 4, 6, 8, 10, 12, 14, 16, 18, 20

DRAIN CHARACTERISTICS AT 125°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −9V

V₉ = −10V

V₉ = −11V

Vᵦₛ = 0V

−Iᴅ (mA): 2, 4, 6, 8, 10, 12, 14, 16, 18, 20

DRAIN CHARACTERISTICS AT −55°C

−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

Vᵦₛ = 0V

V₉ = −5V

V₉ = −9V

V₉ = −10V

V₉ = −6V

V₉ = −7V

V₉ = −11V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT 25°C
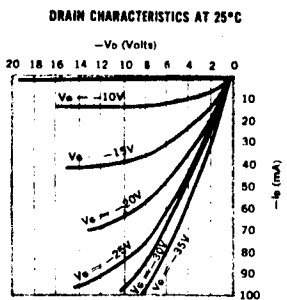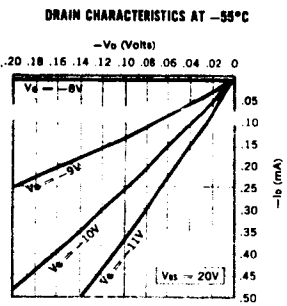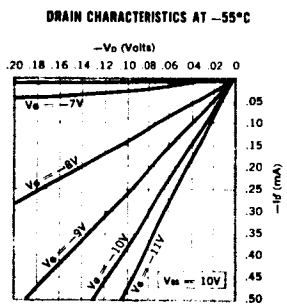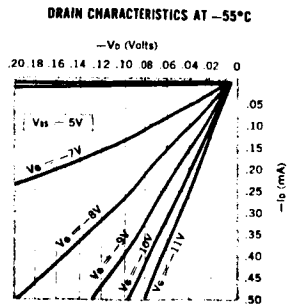
−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

V₉ = −5V

V₉ = −10V

Vᵦₛ = 0V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT 125°C

−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

V₉ = −5V

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −11V

Vᵦₛ = 0V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT −55°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

Vᵦₛ = 0V

V₉ = −5.5V

−Iᴅ (mA): .01, .02, .03, .04, .05, .06, .07, .08, .09, .10

Vₛ in .05 V Steps

DRAIN CHARACTERISTICS AT 25°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

V₉ = −4.5V

−Iᴅ (mA): .01, .02, .03, .04, .05, .06, .07, .08, .09, .10

Vₛ = 0V, .05 V Steps

DRAIN CHARACTERISTICS AT 125°C

−Vᴅ (Volts)

20 18 16 14 12 10 8 6 4 2 0

V₉ = −4.5V

−Iᴅ (mA): .01, .02, .03, .04, .05, .06, .07, .08, .09, .10

Vₛ = 0V, .05 V Steps

DRAIN CHARACTERISTICS AT −55°C

−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

Vᵦₛ = 2V

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −10V

V₉ = −11V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT 25°C

−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

V₉ = −5V

V₉ = −10V

V₉ = −5V

V₉ = −7V

V₉ = −8V

V₉ = −11V

Vᵦₛ = 2V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT 125°C

−Vᴅ (Volts)

.20 .18 .16 .14 .12 .10 .08 .06 .04 .02 0

V₉ = −6V

V₉ = −7V

V₉ = −8V

V₉ = −9V

V₉ = −10V

V₉ = −11V

Vᵦₛ = 2V

−Iᴅ (mA): .05, .10, .15, .20, .25, .30, .35, .40, .45, .50

DRAIN CHARACTERISTICS AT −55°C

DRAIN CHARACTERISTICS AT −55°C

DRAIN CHARACTERISTICS AT −55°C

DRAIN CHARACTERISTICS AT 25°C

DRAIN CHARACTERISTICS AT 25°C

DRAIN CHARACTERISTICS AT 25°C

DRAIN CHARACTERISTICS AT 25°C

DRAIN CHARACTERISTICS AT 125°C

DRAIN CHARACTERISTICS AT 125°C

DRAIN CHARACTERISTICS AT 125°C

0467-98N

MOTOROLA

2N4351

SILICON N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

N-CHANNEL
INSULATED GATE

FIELD-EFFECT
TRANSISTOR

AUGUST 1966 — DS 5179

. . . designed for enhancement-mode operation in low-power switching applications.

- Low Drain-Source Resistance
  $r_{ds(on)} = 300$ ohms max
- Low Reverse Transfer Capacitance
  $C_{rss} = 2.5$ pF max
- Guaranteed Switching Limits
  t_{d1}, t_r, t_{d2}, t_f

MAXIMUM RATINGS (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	+35	Vdc
Gate-Source Voltage	V_{GS}	±35	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation at $T_C = 25°C$ Derate about 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

HANDLING CONSIDERATIONS:

Insulated gate field-effect transistors, due to their extremely high input resistance, are subject to potential damage by the accumulation of excess static charge. To avoid possible damage to the devices while handling, testing, or in actual operation, the following procedure should be followed:
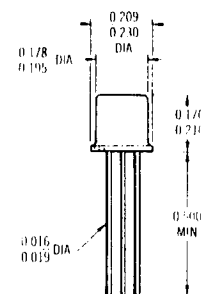
1. The leads of the devices should remain wrapped in the shipping foil except when being tested or in actual operation to avoid the build-up of static charge.
2. Avoid unnecessary handling; when handled, the devices should be picked up by the can instead of the leads.
3. The devices should not be inserted or removed from circuits with the power on as transient voltages may cause permanent damage to the devices.

MOTOROLA Semiconductor Products Inc. (M) A SUBSIDIARY OF MOTOROLA INC.

CAL CHARACTERISTICS (T$_A$ = 25°C unless otherwise noted)

nected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
ACTERISTICS					
Source Breakdown Voltage (10 µA, V$_{GS}$ = 0)	--	V$_{(BR)DSS}$	25	-	V dc
Leakage Current (V$_{GS}$ = 25 V, V$_{DS}$ = 0)	--	I$_{GSS}$	---	10	pAdc
Zero-Gate Voltage Drain Current (V$_{DS}$ = 10 V, V$_{GS}$ = 0)	--	I$_{DSS}$	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V$_{DS}$ = 10 V, I$_D$ = 10 µA)	--	V$_{GS(TH)}$	1.0	5	Vdc
"ON" Drain Current (V$_{GS}$ = 10 V, V$_{DS}$ = 10 V)	3	I$_{D(on)}$	3	--	mAdc
Drain-Source "ON" Voltage (I$_D$ = 2 mA, V$_{GS}$ = 10 V)	--	V$_{DS(on)}$	---	1.0	V
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V$_{GS}$ = 10 V, I$_D$ = 0, f = 1 kHz)	1	r$_{ds(on)}$	—	300	ohms
Forward Transfer Admittance (V$_{DS}$ = 10 V, I$_D$ = 2 mA, f = 1 kHz)	1	|y$_{fs}$|	1000	--	µmho
Reverse Transfer Capacitance (V$_{DS}$ = 0, V$_{GS}$ = 0, f = 140 kHz)	2	C$_{rss}$	—	2.5	pF
Input Capacitance (V$_{DS}$ = 10 V, V$_{GS}$ = 0, f = 140 kHz)	2	C$_{iss}$	—	5.5	pF
Drain-Substrate Capacitance (V$_{D(SUB)}$ = 10 V, f = 140 kHz)	--	C$_{d(sub)}$	—	4.0	pF

SWITCHING CHARACTERISTICS

Turn-On Delay		6, 10	t$_{d1}$	—	45	ns
Rise Time	I$_D$ = 2 mA, V$_{DD}$ = 10 V,	7, 10	t$_r$	—	65	ns
Turn-Off Delay	V$_{GS}$ = 10 V. R$_D$ = R$_S$ = 4.5 k ohms	8, 10	t$_{d2}$	—	35	ns
Fall Time	(See Figure 10; Times Circuit Determined)	9, 10	t$_f$	—	75	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

FIGURE 2 — CAPACITANCE

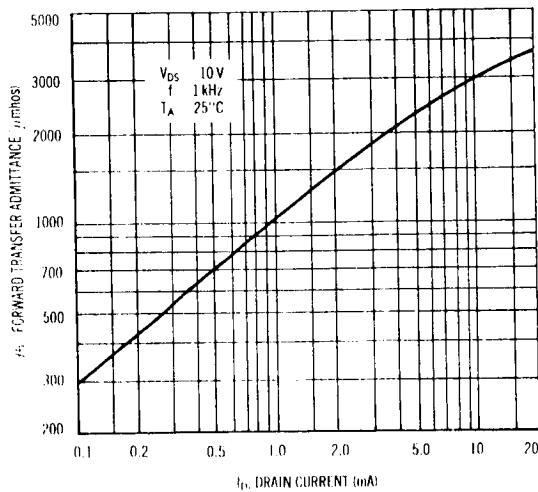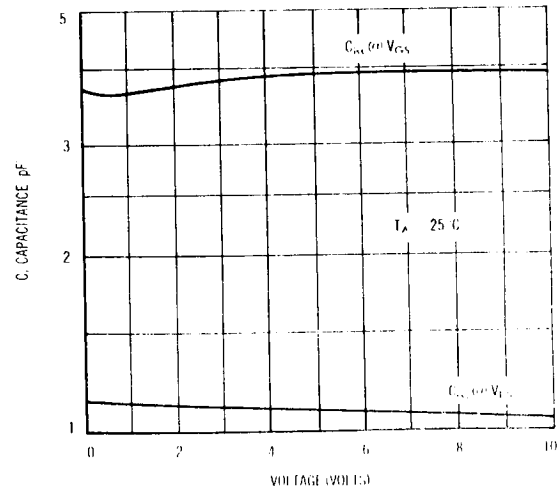**MOTOROLA** *Semiconductor Products Inc.* • • • • • • • • • • • • • • • •

2N4351
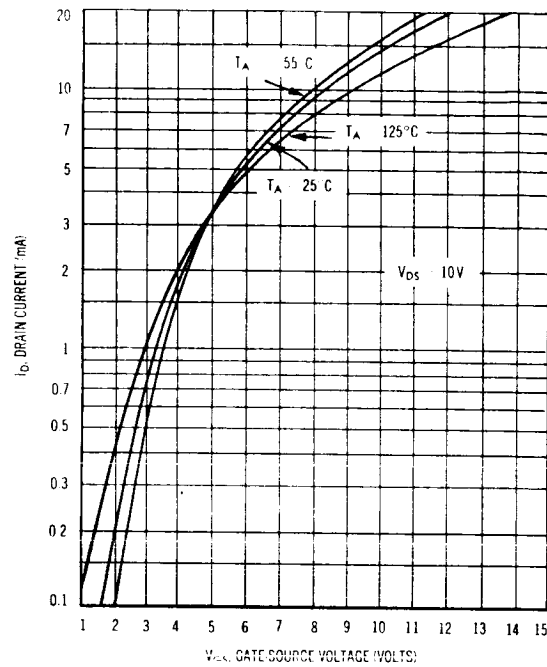
FIGURE 3 — TRANSFER CHARACTERISTICS

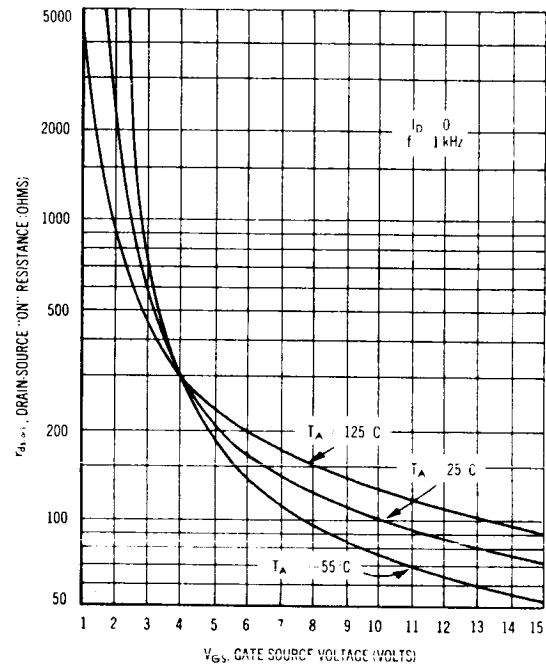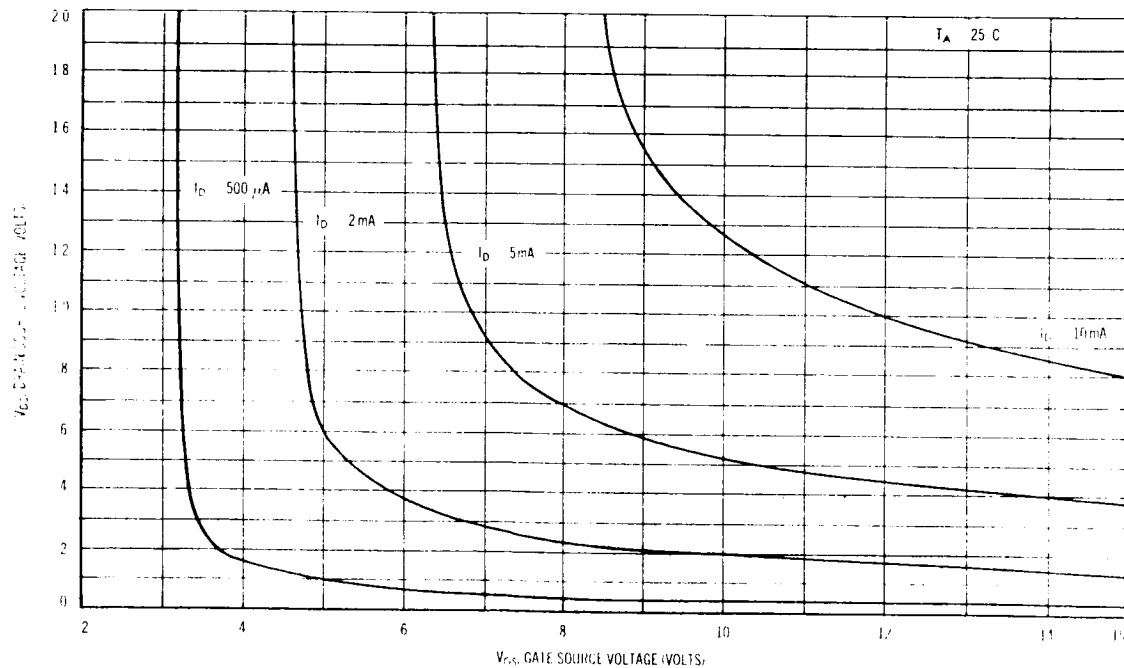FIGURE 4 — DRAIN-SOURCE "ON" RESISTANCE

FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE

MOTOROLA *Semiconductor Products Inc.*

SWITCHING CHARACTERISTICS
($T_A = 25°C$)
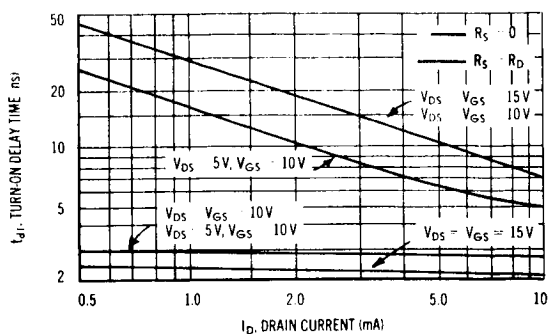
FIGURE 6 — TURN-ON DELAY TIME
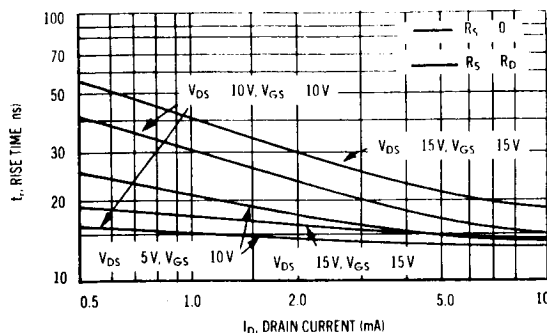

FIGURE 7 — RISE TIME
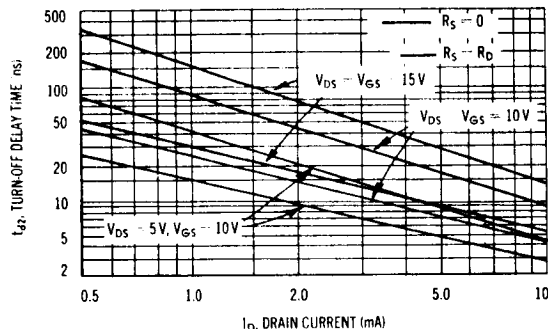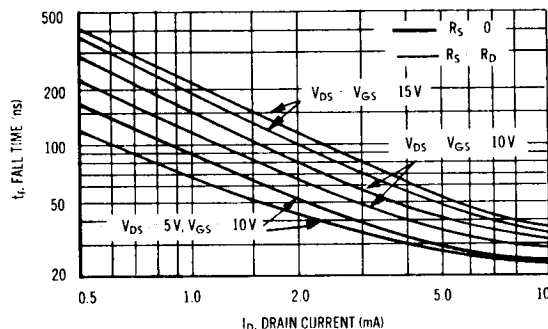

FIGURE 8 — TURN-OFF DELAY TIME
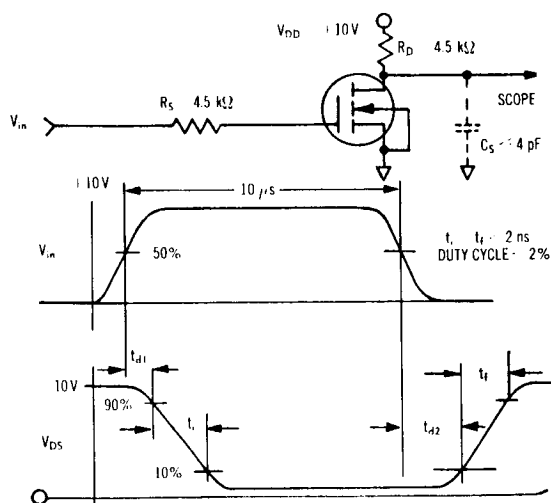

FIGURE 9 — FALL TIME

FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS

The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance (C_{gs}, C_{iss}, C_{rss}) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.
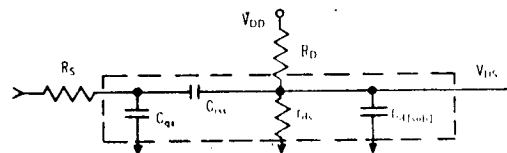
During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed. *

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 11 — SWITCHING CIRCUIT with IGFET EQUIVALENT MODEL

JUNE 1965 SL 6

FI0049
DUAL P-CHANNEL MOS FIELD-EFFECT TRANSISTOR
DIFFUSED SILICON PLANAR II DEVICE

GENERAL DESCRIPTION The FI0049 is a silicon Planar II (Note 1) integrated dual-drain MOS Field Effect Transistor designed primarily for chopper applications and multiplex or commutator switches. The monolithic device can be used in various configurations to form series, shunt, series-shunt choppers and dual-input switches. For low-level applications, the zero offset voltage now permits microvolt chopping with a solid-state device.

PHYSICAL DIMENSIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-65°C to +175°C

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature	(Note 3)	1.7 Watts
at 25°C Ambient Temperature	(Note 3)	0.60 Watt

Maximum Voltages and Current

V_{DSS}	Drain to Source Voltage	-30 Volts
V_{SDS}	Source to Drain Voltage	-30 Volts
V_{DG}	Drain to Gate Voltage	±25 Volts
V_{GS}	Gate to Source Voltage	±25 Volts
V_{GB}	Gate to Body Substrate Voltage	-30 to 0 Volts
I_D	Drain Current	200 mA

ELECTRICAL CHARACTERISTICS
(25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Single Device Min.	Typ.	Max.	Paralleled Device Min.	Typ.	Max.	Units	Test Conditions
I_{DSS}	Drain Leakage Current						1.0	nA	$V_{GS} = 0$ $V_{DS} = -20$ V
I_{SDS}	Source Leakage Current						1.0	nA	$V_{DG} = 0$ $V_{SD} = -20$ V
BV_{DSS}	Drain Breakdown Voltage	-30	-50		-30	-50		Volts	$V_{GS} = 0$ $I_D = 1.0$ μA
BV_{SDS}	Source Breakdown Voltage	-30	-50		-30	-50		Volts	$V_{GD} = 0$ $I_S = 1.0$ μA
$I_D(on)$	Drain On Current	10		50	20		100	mA	$V_{DS} = -20$V $V_{GS} = -15$ V
R_{GS}	Gate Resistance	10^{13}	10^{15}		10^{13}			Ohms	$V_{GS} = V_{GD} = -15$ V
V_{GS}	Gate Threshold Voltage	-3.0		-6.0	-3.0		-6.0	Volts	$V_{DG} = 0$ $I_D = 10$ μA
r_o	Dynamic "ON" Resistance (f = 1.0 Kc)		270	500		135	250	Ohms	$V_{DS} = 0$ $V_{GS} = -15$ V
$gm(Y_{fs})$	Forward Transadmittance (f = 1.0 Kc)	2000			4000			μmhos	$V_{DS} = -20$V $V_{GS} = -15$ V
r_d	Dynamic Drain Resistance (f = 1.0 Kc)		125			70		Kohms	$V_{DS} = -20$V $V_{GS} = -15$ V
C_{iss}	Input Capacity (f = 1.0 Mc)		5.0			10		pf	$V_{DS} = -20$V $V_{GS} = -15$ V
C_{dg}	Drain to Gate Capacity (f = 1.0 Mc)		0.7			1.2		pf	$V_{DS} = -20$V $V_{GS} = -15$ V

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NOTES:

(1) PLANAR II is the process which prevents ion migration in planar oxides under the influence of heavy (e.g., 2×10^6 volts/cm) electric fields.

(2) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(3) These ratings give a maximum junction temperature of 175 C and junction-to-case thermal resistance of 88.2 C/Watt (derating factor of 11.3 mW/ C), junction-to-ambient thermal resistance of 250 C/Watt (derating factor of 4.0 mW/ C).

FAIRCHILD SEMICONDUCTOR

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING
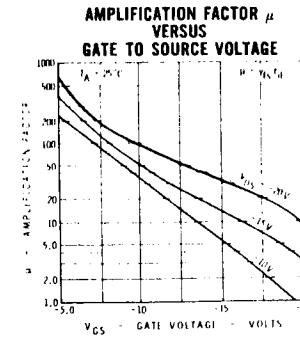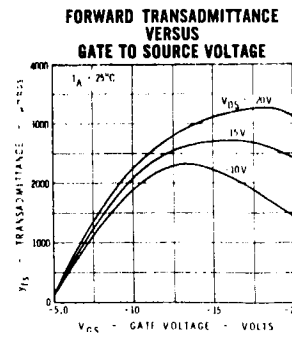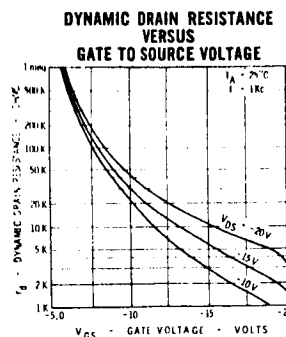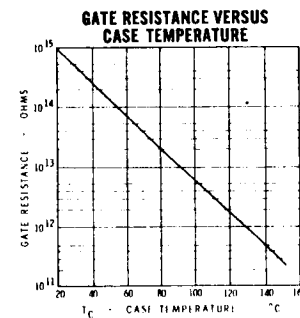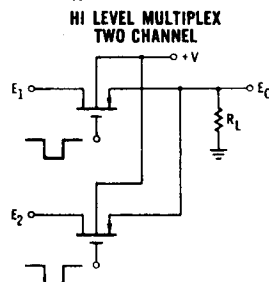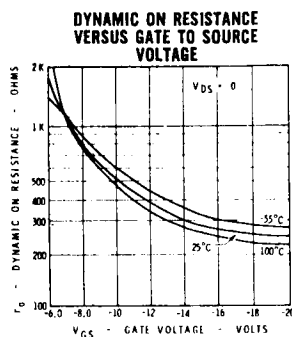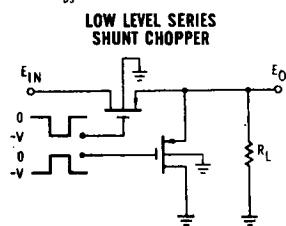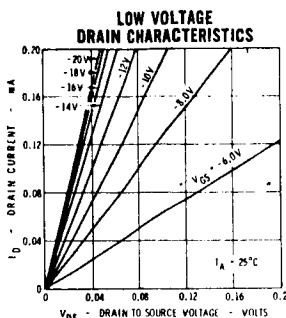
FAIRCHILD TRANSISTOR FI0049

HANDLING INSTRUCTIONS

This is an insulated gate device wherein the insulation is a very thin layer of glass (Si O_2) between the control (gate) electrode and the area beneath. Due to low capacity (C_{gs}) and high-leakage resistance (R_{GS}) of the gate, slight electrostatic charges can result in large voltages capable of damaging the dielectric.

Storage: All six leads should be in contact with each other.

Testing: Grasp the test chassis prior to insertion of the device into any circuit or test equipment. Additional precautions should be taken to ground all soldering iron tips, etc.

TYPICAL ELECTRICAL CHARACTERISTICS

LOW VOLTAGE DRAIN CHARACTERISTICS

DYNAMIC ON RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE OFF RESISTANCE VERSUS CASE TEMPERATURE

LOW LEVEL SERIES SHUNT CHOPPER

HI LEVEL MULTIPLEX TWO CHANNEL

ANALOG SWITCH

DRAIN CHARACTERISTICS

GATE TRANSFER CHARACTERISTICS

GATE RESISTANCE VERSUS CASE TEMPERATURE

DYNAMIC DRAIN RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

AMPLIFICATION FACTOR μ VERSUS GATE TO SOURCE VOLTAGE

Fairchild cannot assume responsibility for use of any circuitry described. No circuit patent licenses are implied.

0467-104N

2N4066 · 2N4067
DUAL P-CHANNEL MOS FIELD-EFFECT TRANSISTORS
DIFFUSED SILICON PLANAR II DEVICES

- ZERO OFF-SET VOLTAGE
- HIGH FIGURE OF MERIT -- $Y_{fs}/C_{iss} = 600$ μmhos/pF TYPICAL
- LOW ON-RESISTANCE -- $r_{ds(on)} = 250$ Ω Max.
- HIGH Y_{fs} -- 2500 μmhos Min. @ 25°C
  -- 1750 μmhos Min. @ 100°C
- LOW LEAKAGE -- $I_{G(f)} = 2.5$ pA Max.
  -- $I_{DSS} = 1.0$ nA Max.

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-76) outline

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	−65°C to +175°C
Lead Temperature (Soldering, 10 s time limit)	+260°C Maximum
Total Dissipation at 25°C Case Temperature (Note 2)	1.7 Watts
at 25°C Ambient Temperature (Note 2)	0.6 Watt

Maximum Voltages and Currents

V_{DSS}	Drain to Source Voltage	−30 Volts
V_{SDS}	Source to Drain Voltage	−30 Volts
V_{GD}	Gate to Drain Voltage	±25 Volts
V_{GS}	Gate to Source Voltage	±25 Volts
V_{GB}	Gate to Body (Substrate) Voltage	−30 to 0 Volts
I_D	Drain Current	200 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Noted)

SYMBOL	CHARACTERISTIC		2N4066 MIN.	TYP.	MAX.	2N4067 MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
BV_{DSS}	Drain to Source Breakdown Voltage		−30			−30			Volts	$I_D = 10$ μA	$V_{GS} = 0$
BV_{SDS}*	Source to Drain Breakdown Voltage		−30			−30			Volts	$I_S = 10$ μA	$V_{GD} = 0$, $V_{BD} = 0$
I_{DSS}	Zero-Gate Voltage Drain Current			0.05	1.0		0.05	1.0	nA	$V_{DS} = -15$ V	$V_{GS} = 0$
I_{SDS}*	Zero-Gate Voltage Source Current			0.07	1.0		0.07	1.0	nA	$V_{SD} = -15$ V	$V_{GD} = 0$, $V_{BD} = 0$
$I_{G(f)}$	Gate Forward Leakage Current			0.1	2.5		0.1	2.5	pA	$V_{GS} = -25$ V	$V_{DS} = 0$
$V_{GS(th)}$	Gate-Source Threshold Voltage		−3.0	−4.5	−6.0	−3.0	−4.5	−6.0	Volts	$V_{DS} = -15$ V	$I_D = 10$ μA
$I_{D(on)}$	"ON" Drain Current		10	22	50	10	22	50	mA	$V_{DS} = -15$ V	$V_{GS} = -15$ V
$r_{ds(on)}$	Drain Source "ON" Resistance (Single)			300	500		125	250	Ohms	$V_{GS} = -15$ V	$I_D = 0$
	(f = 1.0 kHz)	(Paralleled)		150	250		75	125	Ohms		
Y_{fs}	Forward Transadmittance (Single)		1500	2300		2500	3100		μmhos	$V_{DS} = -15$ V	$V_{GS} = -15$ V
	(f = 1.0 kHz)	(Paralleled)	3000	4600		5000	6200		μmhos		

* Body (substrate) connected to Drain.
Body (substrate) connected to Source for all other parameters.

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 88°C/Watt (derating factor of 11.3 mW/°C); junction-to-ambient thermal resistance of 250°C/Watt (derating factor of 4.0 mW/°C). This is the total allowable power dissipation for both sides.
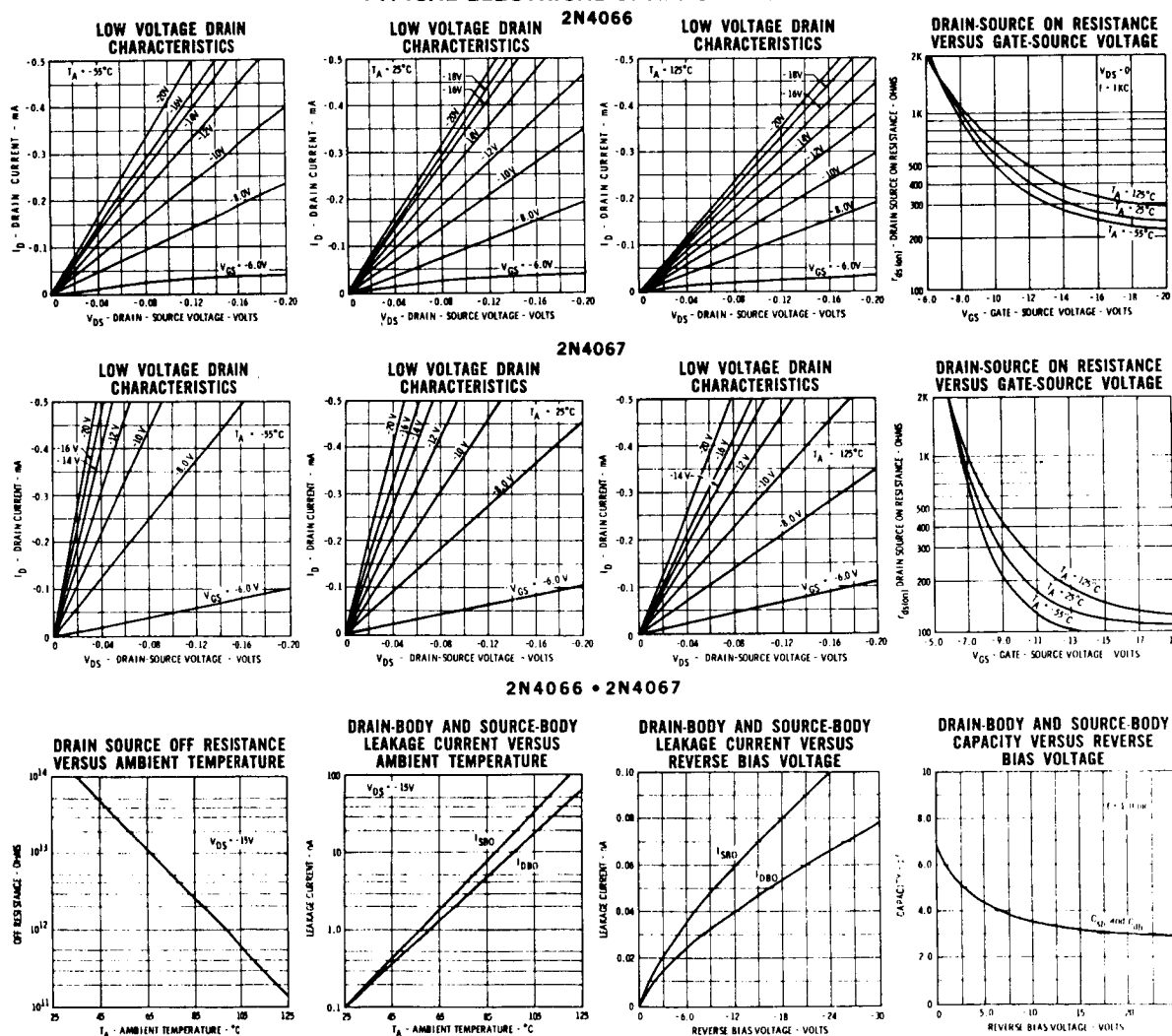
FAIRCHILD

DUAL P-CHANNEL MOS FIELD-EFFECT TRANSISTORS — DIFFUSED SILICON PLANAR II DEVICES

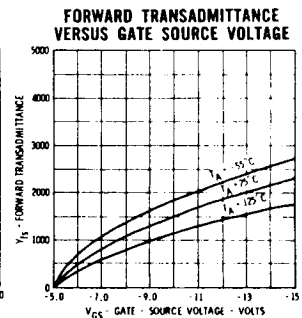## FAIRCHILD TRANSISTORS 2N4066 • 2N4067

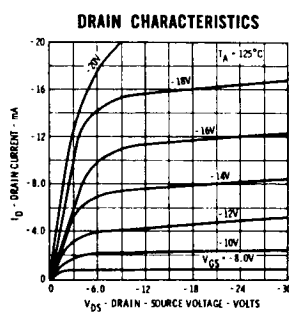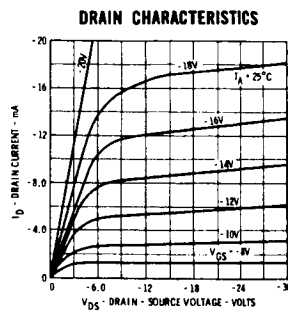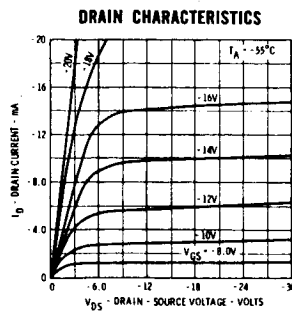**ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Noted)**

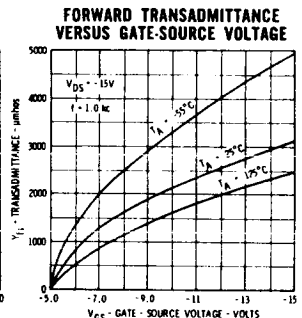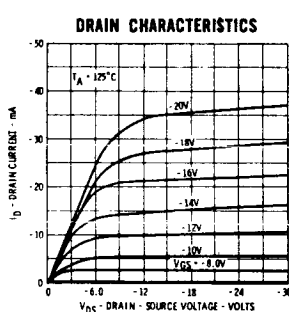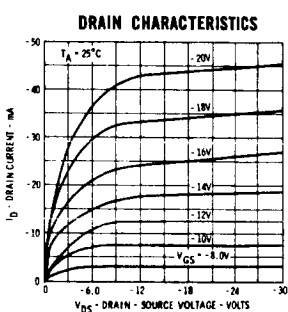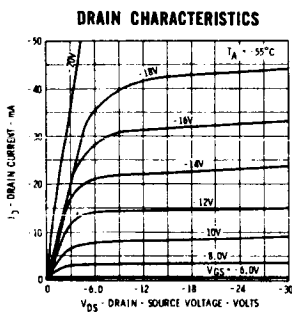| SYMBOL	CHARACTERISTIC	2N4066 MIN.	2N4066 TYP.	MAX.	2N4067 MIN.	2N4067 TYP.	MAX.	UNITS	TEST CONDITIONS	
Y_{fs} (100°C)	Forward Transadmittance (f = 1.0 kHz)	1000	1800		1750	2500		μmhos	$V_{DS} = -15\,V$	$V_{GS} = -15\,V$
Y_{os}	Output Admittance (f = 1.0 kHz)		120	300		120	300	μmhos	$V_{DS} = -15\,V$	$V_{GS} = -15\,V$
C_{iss}	Input Capacitance (f = 1.0 MHz) (Single)		5.5	7.0		5.5	7.0	pF	$V_{DS} = -15\,V$	$V_{GS} = -15\,V$
	(Paralleled)		11	14		11	14	pF		
C_{rss}	Reverse Transfer Capacitance (Single)		0.8	1.5		0.8	1.5	pF	$V_{DS} = 0$	$V_{GS} = 0$
	(f = 1.0 MHz) (Paralleled)		1.6	3.0		1.6	3.0	pF		
I_{DSS} (150°C)	Zero-Gate Voltage Drain Current		0.2	2.0		0.2	2.0	μA	$V_{DS} = -15\,V$	$V_{GS} = 0$
I_{SDS} (150°C)	Zero-Gate Voltage Source Current		0.5	2.0		0.5	2.0	μA	$V_{SD} = -15\,V$	$V_{GD} = 0, V_{SD} = 0$
C_{sb}	Source to Body Capacity (f = 1.0 MHz)		3.0	5.0		3.0	5.0	pF	$V_{DB} = -15\,V$	$V_{GS} = 0, I_{S} = 0$
C_{db}	Drain to Body Capacity (f = 1.0 MHz)		3.0	5.0		3.0	5.0	pF	$V_{DB} = -15\,V$	$V_{GS} = 0, I_{S} = 0$
t_{d}	Delay Time		12	20		12	20	ns	$V_{DD} = -15\,V$ $V_{GS(on)} = -15\,V, R_{L} = R_{G} = 1.4\,K\Omega$	$I_{D(on)} = 10\,mA$
t_{r}	Rise Time		18	30		18	30	ns	$V_{DD} = -15\,V$ $V_{GS(on)} = -15\,V, R_{L} = R_{G} = 1.4\,K\Omega$	$I_{D(on)} = 10\,mA$
t_{off}	Turn Off Time		40	50		40	50	ns	$V_{DD} = -15\,V$ $V_{GS(on)} = -15\,V, R_{L} = R_{G} = 1.4\,K\Omega$	$I_{D(on)} = 10\,mA$

TYPICAL ELECTRICAL CHARACTERISTICS

2N4066

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = -55°C$)

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = 25°C$)

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = 125°C$)

DRAIN-SOURCE ON RESISTANCE VERSUS GATE-SOURCE VOLTAGE

2N4067

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = -55°C$)

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = 25°C$)

LOW VOLTAGE DRAIN CHARACTERISTICS ($T_A = 125°C$)

DRAIN-SOURCE ON RESISTANCE VERSUS GATE-SOURCE VOLTAGE

2N4066 • 2N4067

DRAIN SOURCE OFF RESISTANCE VERSUS AMBIENT TEMPERATURE

DRAIN-BODY AND SOURCE-BODY LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

DRAIN-BODY AND SOURCE-BODY LEAKAGE CURRENT VERSUS REVERSE BIAS VOLTAGE

DRAIN-BODY AND SOURCE-BODY CAPACITY VERSUS REVERSE BIAS VOLTAGE
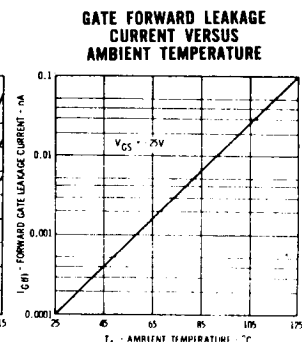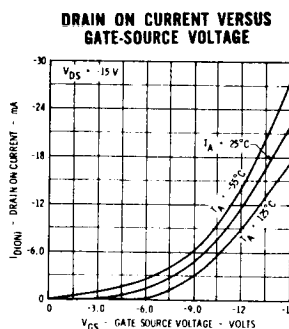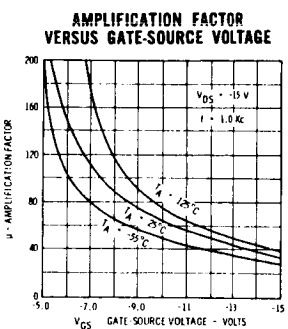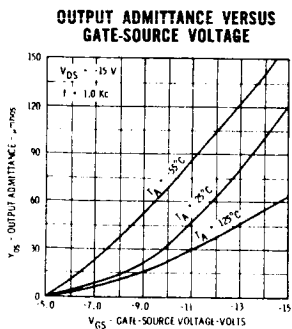
0467-108N

FAIRCHILD TRANSISTORS 2N4066 • 2N4067

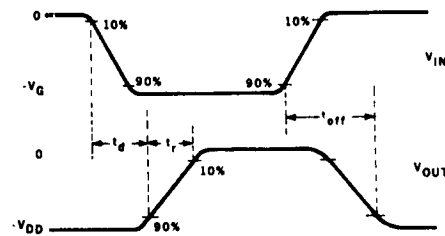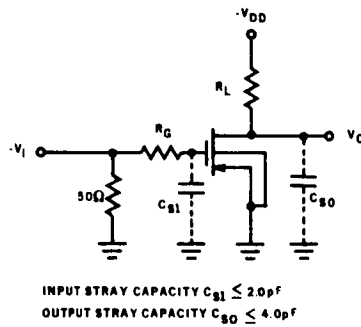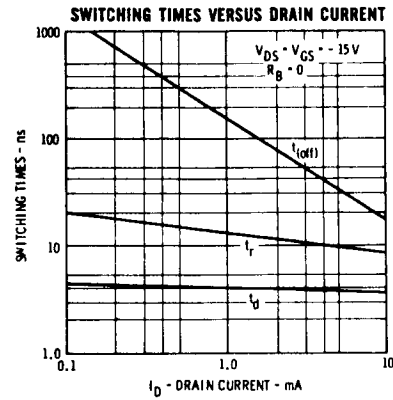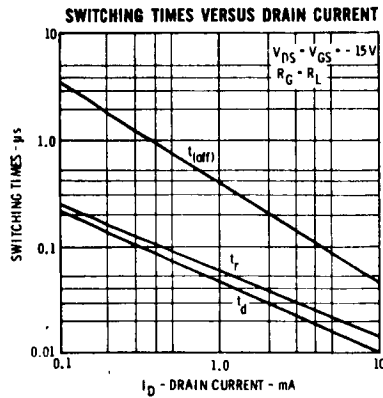### TYPICAL ELECTRICAL CHARACTERISTICS
2N4066

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2N4066 • 2N4067
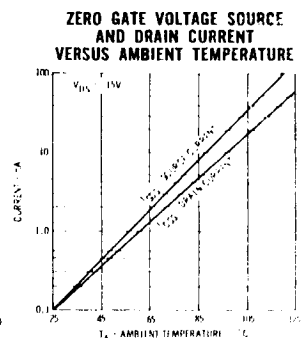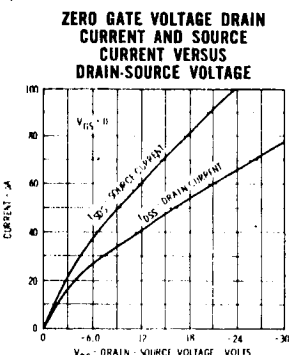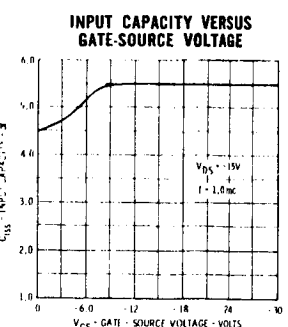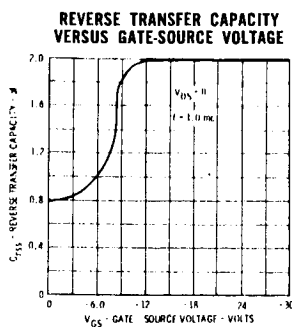
FAIRCHILD TRANSISTORS 2N4066 • 2N4067

SWITCHING CHARACTERISTICS

SWITCHING TIMES VERSUS DRAIN CURRENT

$V_{DS} = V_{GS} = -15V$
$R_G = R_L$

$t_{(off)}$
t_r
t_d

SWITCHING TIMES - μs

I_D - DRAIN CURRENT - mA

SWITCHING TIMES VERSUS DRAIN CURRENT

$V_{DS} = V_{GS} = -15V$
$R_B = 0$

$t_{(off)}$
t_r
t_d

SWITCHING TIMES - ns

I_D - DRAIN CURRENT - mA

INPUT STRAY CAPACITY $C_{S1} \leq 2.0$ pF
OUTPUT STRAY CAPACITY $C_{SO} \leq 4.0$ pF

HANDLING INSTRUCTIONS

This is an insulated gate device wherein the insulation is a very thin layer of glass (SiO_2) between the control (gate) electrode and the area beneath. Due to low capacity (C_{gs}) and high-leakage resistance (R_{GS}) of the gate, slight electrostatic charges can result in large voltages capable of damaging the dielectric.

Storage: All six leads should be in contact with each other.
Testing: Grasp the test chassis prior to insertion of the device into any circuit or test equipment.
      Additional precautions should be taken to ground all soldering iron tips, etc.

FAIRCHILD
SEMICONDUCTOR

0467-10FN

RCA SILICON INSULATED-GATE FIELD-EFFECT ("MOS") TRANSISTOR

(RCA) 3N128

RCA-3N128 (formerly Dev. No.TA2840) is an N-channel, depletion-type silicon insulated-gate field-effect (MOS*) transistor for VHF amplifiers and oscillators in commercial and industrial applications. The 3N128 is also extremely well suited for use in low-frequency amplifier applications requiring a transistor having high power gain and very high input impedance.

Because of its improved transfer characteristic the 3N128 provides substantially better cross-modulation performance in linear-amplifier applications than do conventional (bipolar) transistors.

The insulated gate of the 3N128 is offset towards the source — a feature which provides extremely low feedback capacitance (0.13 pF typ.). The 3N128 is hermetically sealed in a 4-lead metal package.

Application data for RCA-3N128, including biasing requirements, basic circuit configurations, selection of optimum operating point, and methods of automatic gain control are given in RCA Application Note AN-3193, "Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor".

*Metal-Oxide-Semiconductor.

SILICON MOS TRANSISTOR— N-Channel Depletion Type

For Amplifier and Oscillator Applications in Commercial and Industrial VHF Communications Equipment Operating up to 250 MHz

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . + 20 max. V
GATE-TO-SOURCE VOLTAGE, V_{GS}:
  CONTINUOUS . . . . 0, -8 max. V
  INSTANTANEOUS. . . . . ± 15 max. V
DRAIN CURRENT, I_D . . . . Limited by power dissipation
TRANSISTOR DISSIPATION, P_T:
  At Ambient Temperatures up to 100°C. . . . 100 max. mW
AMBIENT-TEMPERATURE RANGE:
  Storage. . . . . -65 to + 125 °C
  Operating . . . . -65 to + 100 °C
LEAD TEMPERATURE (During Soldering):
  At distances not closer than 1/32 inch to seating surface for 10 seconds maximum . . 265 max. °C

Features:

- High input resistance —
  $r_{GS} = 10^{14}$ Ω typ.
- Low gate leakage current —
  $I_{GSS} = 0.1$ pA typ.
- Low feedback capacitance —
  $C_{rss} = 0.13$ pF typ.
- High forward transconductance —
  $g_{fs} = 7300$ μmho typ.
- High vhf power gain —
  $G_{PS} = 18$ dB typ. at 200 MHz
- Low vhf noise figure —
  NF = 4 dB typ. at 200 MHz
- Exceptionally good cross-modulation characteristics

L_1 = 4-1/2 turns #20 AWG wire, 3/16" dia.,
approx. 1/2" long, tapped 1 turn from ground end.

L_2 = 3-1/2 turns #20 AWG wire, 3/8" dia.,
approx. 1/2" long.

* Leadless-type disc capacitor.

▲ Neutralization fixed for a Transistor having a
Typical value of C_{rss} (0.13 pF)

**Fig.1 - Test Circuit used to Measure 200-MHz Power
Gain and Noise Figure.**

* See Fig.1 for Circuit.
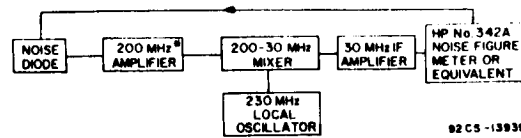
Fig.2 - Noise-Figure Measurement Setup.

ELECTRICAL CHARACTERISTICS: (At T_A = 25°C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	-	10,000	-	μmho
		V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7300	12,000	μmho
Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V	-	0.1	50	pA
Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.8	-	pF
Small-Signal Short-Circuit Reverse Transfer Capacitance*	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	0.13	0.2	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	1.4	-	pF
Gate Leakage Resistance	r_{GS}	V_{DS} = 0, V_{GS} = -8 V	-	10^{14}	-	Ω
Drain-to-Source Channel Resistance	r_{ds}	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
Pinch-Off Voltage	V_P	I_D = 50 μA, V_{DS} = 15 V	-	-3.5	-8	V
Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	30	mA
Power Gain (see Fig.1)	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	14.5	18	-	dB
Noise Figure (see Figs.1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	4	5	dB

*Three-Terminal Measurement: Source Returned to Guard Terminal.   **Pulse Test: Pulse Duration 20 ms max. Duty Factor $\leq$ 0.15.

HANDLING AND OPERATING CONSIDERATIONS

CAUTION

RCA-3N128, like conventional (bipolar) high-frequency silicon transistors, is susceptible to the detrimental effects of high-potential electrostatic discharges applied to its input terminals.

The polystyrene insulating snow, commonly used as a convenient carrying tray for semiconductor devices, can acquire high static charges and should not be used unless it has been specially treated to make it electrically conductive (R ≥ 10 kΩ/in³).

To avoid the possibility of subjecting these devices to high ac voltages that may be present on the tips of soldering irons, some means for grounding these tips should be provided.

RCA 3N128 should never be inserted in or removed from circuits with the power on because transient voltages may permanently damage the device. AC-operated power supplies for the 3N128 should also have provision for suppression of transients during turn-on and turn-off. If such suppression is not provided, the following procedure should be used in applying power to the 3N128.

1 – Before inserting the 3N128 in the equipment turn ac line switch on and reduce the dc output of the power supply to zero.

2 – Insert the 3N128.

3 – Increase the dc supply voltage to the desired value.

This procedure should be reversed when the 3N128 is taken out of the equipment.

TYPICAL CHARACTERISTICS
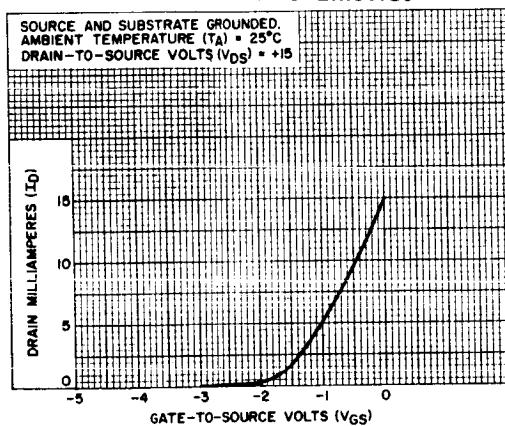
Fig.3 - Drain Current vs Gate-to-Source Voltage.
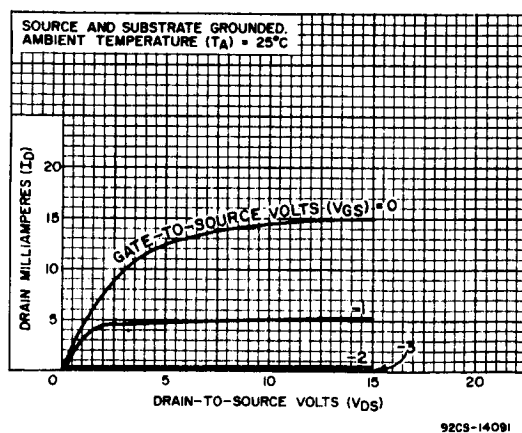
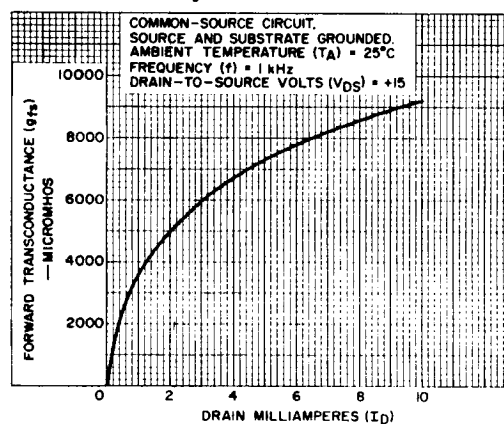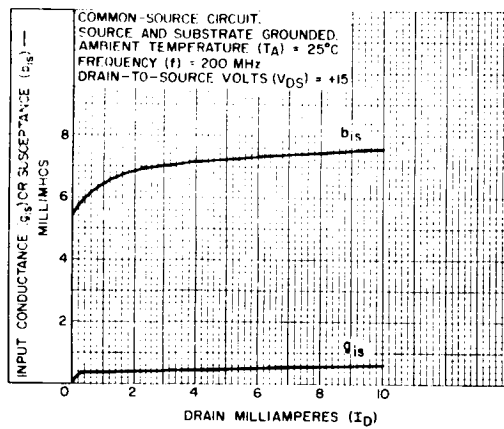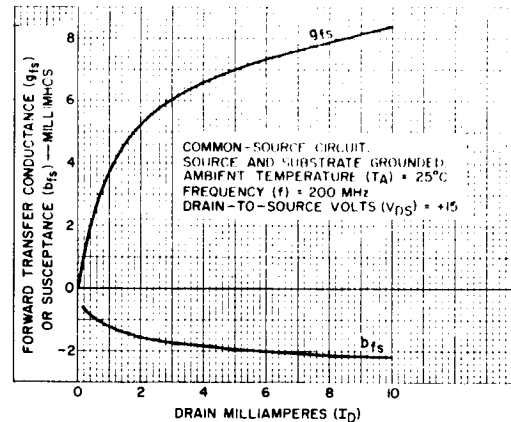Fig.4 - Drain Current vs Drain-to-Source Voltage.

Fig.5 - 1-kHz Forward Transconductance vs Drain Current.

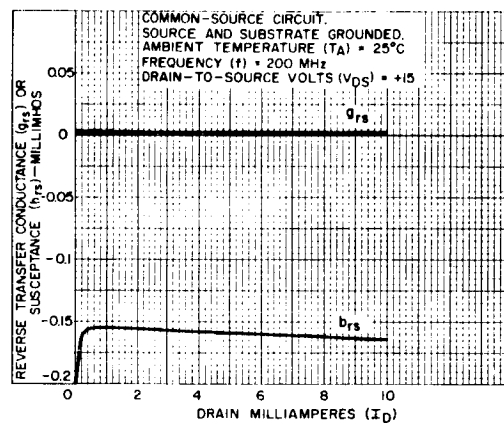## TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y)
COMPONENTS vs DRAIN CURRENT
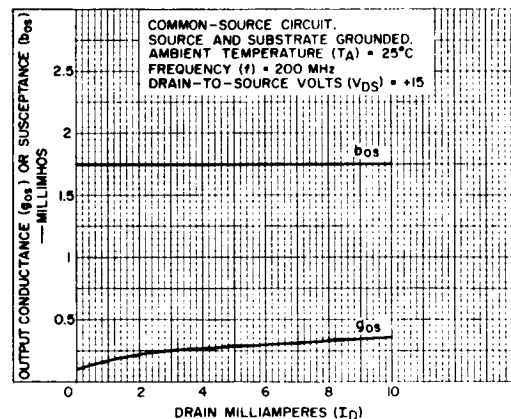

Fig.6 - Input Admittance (Y_{is}) Components.

Fig.7 - Forward Transadmittance (Y_{fs}) Components.

Fig.8 - Reverse Transadmittance (Y_{rs}) Components.

Fig.9 - Output Admittance (Y_{os}) Components.

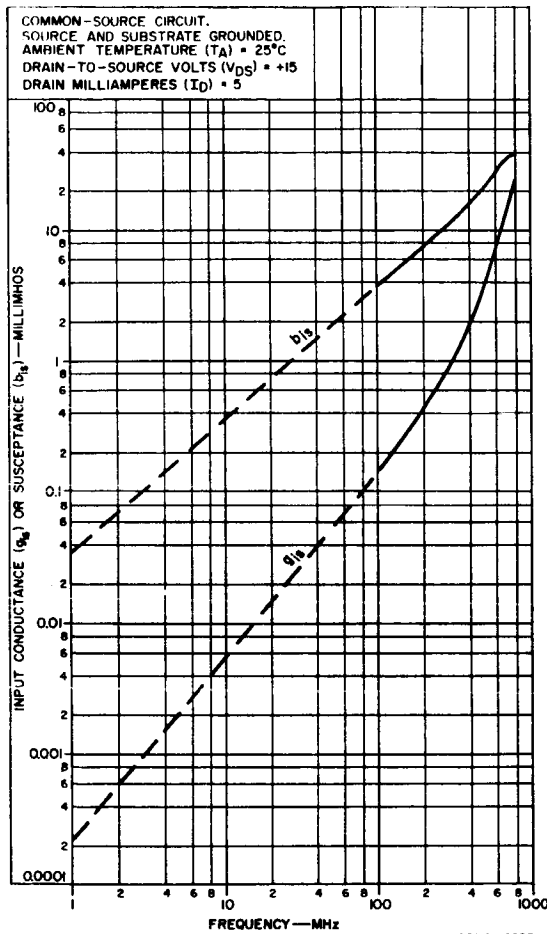## TYPICAL COMMON-SOURCE ADMITTANCE (Y) COMPONENTS
vs FREQUENCY

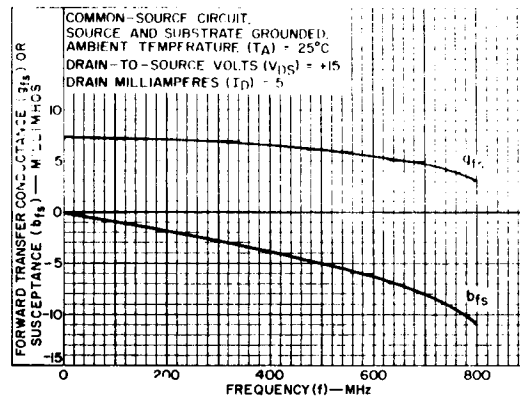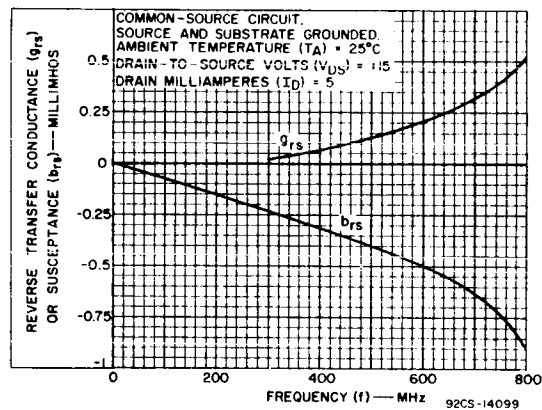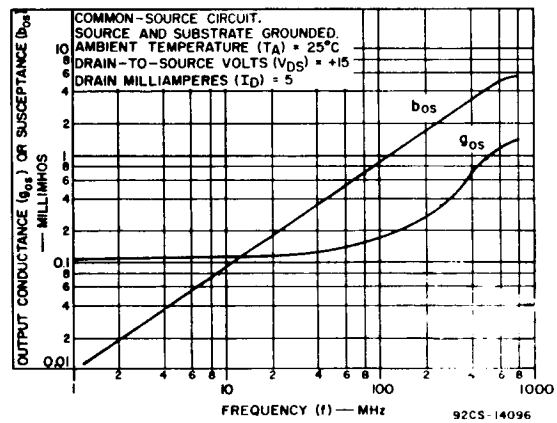Fig.10 - Input Admittance (Y$_{is}$) Components.

Fig.11 - Forward Transadmittance (Y$_{fs}$) Components.

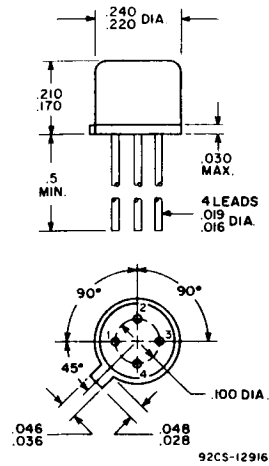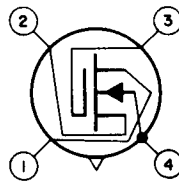Fig.12 - Reverse Transadmittance (Y$_{rs}$) Components.

Fig.13 - Output Admittance (Y$_{os}$) Components.

DIMENSIONAL OUTLINE

92CS-12916

Dimensions in Inches

TERMINAL DIAGRAM

1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate)
    and Case